

AG10KSDE176

DATASHEET

CONFIDENTIAL

AGM AG10KSDE176 是由 AGM FPGA AG10K 与 SDRAM 叠封集成的芯片，具有 AG10K FPGA 的可编程功能，提供更多可编程 IO，同时内部连接大容量 SDRAM。

- **FPGA 外部管脚输出**

EQFP176 封装底部 Pad 为 GND，管脚说明请见下表：

Bank	Pin Name	Function
B1	Pin_1	IO
B1	Pin_2	IO
B1	Pin_3	IO
B1	Pin_4	IO
B1	Pin_5	Ground
B1	Pin_6	IO
B1	Pin_7	VDDC Power 1.2V
B1	Pin_8	IO (DATA1, ASD0)
B1	Pin_9	IO (nCS0)
B1	Pin_10	IO
B1	Pin_11	nSTATUS
B1	Pin_12	Ground
B1	Pin_13	IO
B1	Pin_14	IO
B1	Pin_15	DCLK
B1	Pin_16	IO (DATA0)
B1	Pin_17	nCONFIG
B1	Pin_18	TDI
B1	Pin_19	TCK
B1	Pin_20	VDDI01 Power 3.3V

B1	Pin_21	TMS
B1	Pin_22	TD0
B1	Pin_23	CLK1
B2	Pin_24	CLK2
B2	Pin_25	CLK3
B2	Pin_26	I0
B2	Pin_27	I0
B2	Pin_28	VDDI02 Power 3.3V
B2	Pin_29	Ground
B2	Pin_30	VDDC Power 1.2V
B2	Pin_31	I0
B2	Pin_32	I0
B2	Pin_33	I0
B2	Pin_34	I0
B2	Pin_35	I0
B2	Pin_36	I0
B2	Pin_37	I0
B2	Pin_38	I0
B2	Pin_39	I0
B2	Pin_40	I0
B2	Pin_41	Ground
B2	Pin_42	I0
B2	Pin_43	PLL0 analog power 2.5V
B2	Pin_44	PLL0 digital ground
B2	Pin_45	PLL0 digital power 1.2V
B3	Pin_46	I0

B3	Pin_47	IO
B3	Pin_48	IO
B3	Pin_49	IO
B3	Pin_50	IO
B3	Pin_51	Ground
B3	Pin_52	IO
B3	Pin_53	IO
B3	Pin_54	VDDC Power 1.2V
B3	Pin_55	Ground
B3	Pin_56	IO
B3	Pin_57	IO
B3	Pin_58	IO
B3	Pin_59	IO
B3	Pin_60	IO
B3	Pin_61	IO
B3	Pin_62	IO
B3	Pin_63	IO
B3	Pin_64	IO
B3	Pin_65	IO
B3	Pin_66	VDDI03 Power 3.3V
B3	Pin_67	IO
B3	Pin_68	Ground
B4	Pin_69	Ground
B4	Pin_70	IO
B4	Pin_71	VDDC Power 1.2V
B4	Pin_72	IO

B4	Pin_73	Ground
B4	Pin_74	10
B4	Pin_75	10
B4	Pin_76	10
B4	Pin_77	10
B4	Pin_78	10
B4	Pin_79	10
B4	Pin_80	10
B4	Pin_81	10
B4	Pin_82	VDDI04 Power 3.3V
B4	Pin_83	10
B4	Pin_84	Ground
B4	Pin_85	10
B4	Pin_86	10
B4	Pin_87	10
B4	Pin_88	10
B5	Pin_89	10
B5	Pin_90	10
B5	Pin_91	10
B5	Pin_92	10
B5	Pin_93	10
B5	Pin_94	10
B5	Pin_95	10
B5	Pin_96	10
B5	Pin_97	VDDC Power 1.2V
B5	Pin_98	10

B5	Pin_99	Ground
B5	Pin_100	I0
B5	Pin_101	I0
B5	Pin_102	I0
B5	Pin_103	I0
B5	Pin_104	I0
B5	Pin_105	VDDI05 Power 3.3V
B5	Pin_106	I0
B5	Pin_107	I0
B5	Pin_108	I0
B5	Pin_109	I0
B5	Pin_110	I0
B5	Pin_111	CLK7
B5	Pin_112	CLK6
B5	Pin_113	Ground
B6	Pin_114	CLK5
B6	Pin_115	CLK4
B6	Pin_116	CONF_DONE
B6	Pin_117	Ground
B6	Pin_118	MSEL1
B6	Pin_119	I0
B6	Pin_120	I0
B6	Pin_121	VDDC Power 1.2V
B6	Pin_122	I0
B6	Pin_123	Ground
B6	Pin_124	I0

B6	Pin_125	IO
B6	Pin_126	IO
B6	Pin_127	VDDI06 Power 3.3V
B6	Pin_128	IO
B6	Pin_129	IO
B6	Pin_130	IO
B6	Pin_131	PLL1 analog power 2.5V
B6	Pin_132	PLL1 digital ground
B6	Pin_133	PLL1 digital power 1.2V
B7	Pin_134	IO
B7	Pin_135	IO
B7	Pin_136	IO
B7	Pin_137	IO
B7	Pin_138	Ground
B7	Pin_139	IO
B7	Pin_140	IO
B7	Pin_141	VDDC Power 1.2V
B7	Pin_142	IO
B7	Pin_143	IO
B7	Pin_144	IO
B7	Pin_145	Ground
B7	Pin_146	IO
B7	Pin_147	VDDI07 Power 3.3V
B7	Pin_148	IO
B7	Pin_149	Ground
B7	Pin_150	Ground

B7	Pin_151	IO
B7	Pin_152	IO
B8	Pin_153	IO
B8	Pin_154	IO
B8	Pin_155	Ground
B8	Pin_156	IO
B8	Pin_157	IO
B8	Pin_158	IO
B8	Pin_159	IO
B8	Pin_160	IO
B8	Pin_161	VDDC Power 1.2V
B8	Pin_162	IO
B8	Pin_163	IO
B8	Pin_164	Ground
B8	Pin_165	IO
B8	Pin_166	IO
B8	Pin_167	VDDI08 Power 3.3V
B8	Pin_168	IO
B8	Pin_169	Ground
B8	Pin_170	IO
B8	Pin_171	IO
B8	Pin_172	IO
B8	Pin_173	IO
B8	Pin_174	Ground
B8	Pin_175	IO
B8	Pin_176	IO

- **SDRAM 说明**

内部 SDRAM 为 64Mbit (512K words × 4 banks × 32 bits) 容量。由于 SDRAM 为 3.3V 器件，FPGA 的 VCCIO 也需接 3.3V。

FPGA 的 IO 与 SDRAM 的内部连接，请见下表：

Bank	SDRAM Finger	FPGA Pin Name	Function
B3	/CAS	SDRAM_CAS	I/O
B4	/CS	SDRAM_CS	I/O
B3	/RAS	SDRAM_RAS	I/O
B3	/WE	SDRAM_WE	I/O
B7	A0	SDRAM_A0	I/O
B7	A1	SDRAM_A1	I/O
B7	A2	SDRAM_A2	I/O
B7	A3	SDRAM_A3	I/O
B4	A4	SDRAM_A4	I/O
B4	A5	SDRAM_A5	I/O
B4	A6	SDRAM_A6	I/O
B4	A7	SDRAM_A7	I/O
B4	A8	SDRAM_A8	I/O
B4	A9	SDRAM_A9	I/O
B7	A10	SDRAM_A10	I/O
B7	BA0	SDRAM_BA0	I/O
B8	BA1	SDRAM_BA1	I/O
B3	CKE	SDRAM_CKE	I/O
B8	CLK	SDRAM_CLK	I/O
B2	DQ0	SDRAM_DQ0	I/O

B2	DQ1	SDRAM_DQ1	10
B2	DQ2	SDRAM_DQ2	10
B2	DQ3	SDRAM_DQ3	10
B2	DQ4	SDRAM_DQ4	10
B3	DQ5	SDRAM_DQ5	10
B3	DQ6	SDRAM_DQ6	10
B3	DQ7	SDRAM_DQ7	10
B8	DQ8	SDRAM_DQ8	10
B8	DQ9	SDRAM_DQ9	10
B8	DQ10	SDRAM_DQ10	10
B8	DQ11	SDRAM_DQ11	10
B8	DQ12	SDRAM_DQ12	10
B8	DQ13	SDRAM_DQ13	10
B1	DQ14	SDRAM_DQ14	10
B1	DQ15	SDRAM_DQ15	10
B5	DQ16	SDRAM_DQ16	10
B5	DQ17	SDRAM_DQ17	10
B5	DQ18	SDRAM_DQ18	10
B5	DQ19	SDRAM_DQ19	10
B4	DQ20	SDRAM_DQ20	10
B4	DQ21	SDRAM_DQ21	10
B4	DQ22	SDRAM_DQ22	10
B4	DQ23	SDRAM_DQ23	10
B7	DQ24	SDRAM_DQ24	10

B7	DQ25	SDRAM_DQ25	10
B7	DQ26	SDRAM_DQ26	10
B7	DQ27	SDRAM_DQ27	10
B7	DQ28	SDRAM_DQ28	10
B7	DQ29	SDRAM_DQ29	10
B6	DQ30	SDRAM_DQ30	10
B6	DQ31	SDRAM_DQ31	10
B3	DQM0	SDRAM_DQM0	10
B8	DQM1	SDRAM_DQM1	10
B4	DQM2	SDRAM_DQM2	10
B7	DQM3	SDRAM_DQM3	10

- **配置说明**

AG10K 配置方式支持 JTAG, AS (Master) 和 PS (Slave) 方式, 可通过 MSEL[2..0]选择。其中 MSEL2 和 MSEL0 已在封装内接到 GND, 仅需把外部管脚 MSEL1 按照下表设置, 选择不同配置模式。

配置方式	MSEL1
AS	1
PS	0
JTAG	0/1

● 封装图

