

DATA SHEET

Revision: 1.0

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AGM AG16K PSoC

Low Cost and High Integration PSoC

General Description

AGM AG16K PSoC is targeted to high-volume, cost-sensitive, applications, enabling system designers to meet increasing performance requirements while lowering costs. It is based on AGM PSoC architecture

This device integrate one ARM® Cortex™ core, AGM programmable logic, 12-bit ADC, 64Mbits SDRAM or 128Mbits DDR SDRAM in single device.

The AGM PSoC, its low cost and optimized feature set makes ideal solutions for a wide array of consumer, communications, video processing, test and measurement, and other end-market solutions.

Features

MCU Architecture:

- **One-core ARM® Cortex™:** Working frequency up to 200 MHz
- **On-Chip Memory:** 128Kbytes SRAM
- **I/O Interfaces:**
 - External AHB Slave Interface
 - On-Chip Memory Access Ports
 - UART Interface
 - GPIOs
 - JTAG Debug Ports
 - SPI Flash Interface
- **Interconnect:** ARM AMBA® AHB based

SDRAM:

- 16bits datawidth
- 64Mbits capability
- up to 166MHz working frequency

Analog-to-Digital Converters (ADC) :

- 12bits accuracy
- 1MHz sampling frequency
- On-chip temperature sensing

- Up to 10 channels(include internal temperature sensor channel)

FPGA Architecture:

- High-density architecture with 16K LEs
- M9K embedded memory blocks, up to 504 Kbits of RAM space
- Up to 56 18 x 18-bit embedded multipliers are each configurable as two independent 9 x 9-bit multipliers
- Provides 4 PLLs per device provide clock multiplication and phase shifting
- High-speed differential I/O standard support, including LVDS, RSDS, mini-LVDS, LVPECL
- support DDR, DDR2
- Single-ended I/O standard support, including 3.3V, 2.5V, 1.8V, and 1.5V LVCMOS and LVTTTL
- Flexible device configuration mode: JTAG and AS, PS
- Support remote update, by "dual-boot" like implementation

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1. Feature Summary

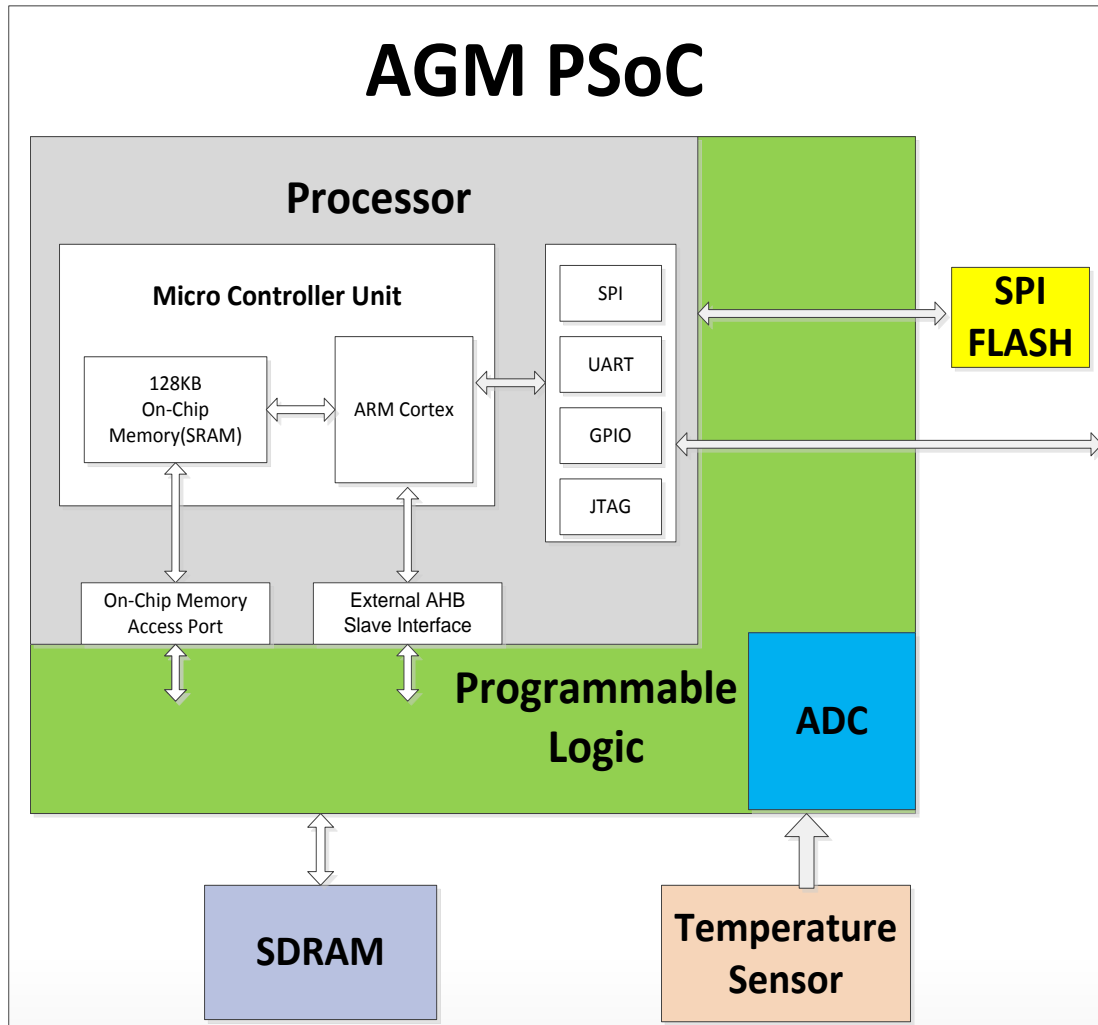
Table 1-1: AGM PSoC

AGM PSoC		
Device Name		AG16K PSoC
MCU	Processor Core	ARM Cortex
	Maximum Frequency	200MHz
	On-Chip Memory(SRAM)	128KBytes
	Interfaces	AHB Master and Slave Interface, On-Chip Memory Access Port, 1 x UART, 24 x GPIOs, 1 x SPI Flash Interface
Memory	Capability	DDR – 128Mbits, SDRAM - 64Mbits
	Datawidth	DDR – 16bits, SDRAM - 32bits
	Max Working Frequency	DDR – 400MHz, SDRAM - 166MHz
FPGA	Logic elements (LEs)	16624
	Embedded memory (Kbits)	504
	Embedded 18 x 18 multipliers	56
	General-purpose PLLs	4
	Global Clock Networks	20
	User I/O Banks	8

Table 1-2: Device-Package Combinations: Maximum I/Os

Device	AG16KSDE176M	AG16KSDE176GM	AG16KSDF256M	AG16KDDF256M
Package	EQFP176	EQFP176	FBGA256	FBGA256
Body Size(mm)	20 x 20	20 x 20	17 x 17	17 x 17
Pitch(mm)	0.4	0.4	1.0	1.0
Max User IO	124	139	152	169

Figure 1-1 illustrates the functional blocks of AGM PSoC.



2. MCU Architecture

2.1. Functional Description

The AGM PSoC device contains an processor, a FPGA, a SDRAM/DDR, an ADC and a Flash in one chip with laminated seal technology.

The AGM PSoC offers the flexibility and scalability of an FPGA, while providing performance, power, and

ease of use typically asPSoCiated with ASIC and ASSPs.

As shown in Figure 1-1, the MCU comprises four major blocks:

- Processor Unit
- On-Chip Memory Access Interface
- External AHB Slave Interface
- I/O peripherals (IOP)

2.2.Processor Unit

The key features of the Processor Unit include:

- 32-bit Micro Processor
- Maximum Frequency: 200MHz
- On-Chip Memory(SRAM): 128Kbytes
- Single cycle multiplication and hardware division
- Integrated nested interrupt controller (NVIC)
- Two timers(each timer can be configured as a 32 bit timer or two 16 bit timers)
- Private Watch Dog timer
- Cortex M3 embedded tracking module (ETM)
- Serial Debug mode (SWP)

2.3.On-Chip Memory Access Interface

The on-chip memory module contains 128 KB of RAM. It is accessed by Micro Processor and programmable logic through AHB bus interconnect.

On-chip memory supports high read and write throughput for RAM access by implementing the RAM as a four-byte memory (32 bits).

Table 2-1 introduces the On-Chip memory access interface port function.

Table 2-1 On-Chip Memory Access Ports

Pin Name	I/O Direction	Function
EXT_RAM_EN	Input	RAM enable, active high
EXT_RAM_WR	Input	RAM write/read control, write — 1 read — 0
EXT_RAM_ADDR[13:0]	Input	RAM address
EXT_RAM_BYTE_EN [3:0]	Input	RAM data byte enable, active high
EXT_RAM_WDATA[31:0]	Input	RAM write data

EXT_RAM_RDATA[31:0]	Output	RAM read data
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2.4. External AHB Slave Interface

The MCU provide another external AHB slave interface for FPGA data communication like as On-Chip memory access interface. The AHB slave interface can support 32-bit write and read data interface for FPGA.

Table 2-2 introduces the external AHB slave ports function.

Table 2-2 External AHB Slave Ports

Pin Name	I/O Direction	Function
HRESP_EXT[1:0]	Input	
HREADY_OUT_EXT	Input	FPGA Slave Ready
HRDATA_EXT[31:0]	Input	FPGA send data to MCU
HTRANS_EXT[1:0]	Output	
HADDR_EXT[31:0]	Output	MCU access address
HWRITE_EXT	Output	Write Enable
HSEL_EXT	Output	
HWDATA_EXT[31:0]	Output	MCU write data to FPGA
HSIZE_EXT[2:0]	Output	
HREADY_IN_EXT	Output	

2.5. I/O peripherals (IOP)

UART Port

The UART controller is a full-duplex asynchronous receiver and transmitter that supports a wide range of programmable baud rates and I/O signal formats. The controller can accommodate automatic parity generation and multi-master detection mode. The controller is structured with separate Rx and Tx data paths.

The UART controller has the following features:

- Programmable baud rate generator
- 64-byte receive and transmit FIFOs
- Programmable protocol:
 - 6, 7, or 8 data bits
 - 1, 1.5, or 2 stop bits
 - Odd, even, space, mark, or no parity
- Parity, framing and overrun error detection
- Line-break generation
- Interrupts generation
- Rx/D and Tx/D modes: Normal/echo and diagnostic loopbacks using the mode

switch

Table 2-3 introduces the UART ports function.

Table 2-3 UART Ports

Pin Name	I/O Direction	Function
UART_RXD	Input	UART Receive Serial Data
UART_CTS_n	Input	Clear to Send
UART_TXD	Output	UART Send Serial Data
UART_RTS_n	Output	Require To Send

SPI Flash Interface

The MCU can use SPI flash interface to access the internal SPI flash, or through FPGA I/O to access other external SPI flash device.

The flash interface has following features :

- 4-bit parallel NOR flash supporting up to 64 MB
- ONFi 1.0 NAND flash support with 1-bit ECC
- 1-bit SPI, 2-bit SPI, 4-bit SPI (quad-SPI) serial NOR flash

Table 2-4 introduces the SPI flash ports function.

Table 2-4 SPI Flash Ports

Pin Name	I/O Direction	Function
FLASH_BIAS[23:0]	Input	Flash offset address
FLASH_SCK	Output	Flash access clock
FLASH_CS_n	Output	Flash chip select, active low
FLASH_IO0_SI	Output	MCU data to flash
FLASH_IO1_SO	Output	
FLASH_IO2_WPn	Output	Flash write protection, active low
FLASH_IO3_HOLDn	Output	Flash hold signal, active low
FLASH_IO0_SI_i	Input	
FLASH_IO1_SO_i	Input	Flash data to MCU
FLASH_IO2_WPn_i	Input	
FLASH_IO3_HOLDn_i	Input	
FLASH_SI_OE	Output	Data in enable, active high
FLASH_SO_OE	Output	Data out enable, active high
WPn_IO2_OE	Output	WP enable, active high
HOLDn_IO3_OE	Output	Hold enable, active high

GPIOs

The GPIOs have following features:

- Up to 24 GPIO signals for device pins routed through FPGA
- Outputs are 3-state capable

The function of each GPIO can be dynamically programmed on an individual or group basis.

Table 2-5 introduces the GPIO ports function.

Table 2-5 GPIO Ports

Pin Name	I/O Direction	Function
GPIO0_I[7:0]	Input	GPIO0 byte data input, nGPEN0 as bit enable
GPIO1_I[7:0]	Input	GPIO1 byte data input, nGPEN1 as bit enable
GPIO2_I[7:0]	Input	GPIO2 byte data input, nGPEN2 as bit enable
GPIO0_O[7:0]	Output	GPIO0 byte data output, nGPEN0 as bit input/output enable, High – GPIO0_I enable, low – GPIO0_O enable
GPIO1_O[7:0]	Output	GPIO1 byte data output, nGPEN1 as bit input/output enable, High – GPIO1_I enable, low – GPIO1_O enable
GPIO2_O[7:0]	Output	GPIO2 byte data output, nGPEN2 as bit input/output enable, High – GPIO2_I enable, low – GPIO2_O enable
nGPEN0[7:0]	Output	GPIO0 byte output enable
nGPEN1[7:0]	Output	GPIO1 byte output enable
nGPEN2[7:0]	Output	GPIO2 byte output enable
O_INI_IP	Output	Active high, MCU initial process is on going and user can't access MCU

Debug Port(JTAG and SWD)

This debug port(JTAG and SWD) can be used to debug MCU code through FPGA IO. User can use

J-LINK to debug the application. Table 2-6 introduces the JTAG port.

Table 2-6 Debug Ports

Pin Name	I/O Direction	Function
JTCK	Input	JTAG clock input
JTDI	Input	JTAG data input
JTMS	Input	JTAG mode input
JTDO	Output	JTAG data output
SWDO	Output	SWD Output
SWDOEN	Output	SWD Output En

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3. Memory

3.1. Functional Description

DDR: The integrated DDR is a CMOS Double Data Rate synchronous dynamic random access memory (DDR SDRAM); organized as 2M words \times 4 banks \times 16 bits. It delivers a data bandwidth of up to 400M words per second.

SDRAM: The integrated SDRAM is a high speed synchronous dynamic random access memory (SDRAM), organized as 1024K words \times 4 banks \times 16 bits(64Mbits). The SDRAM delivers a data bandwidth of up to 166M words per second.

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4. Analog-to-Digital Converters (ADC)

4.1. Functional Description

The Analog-to-Digital Converters (ADC) is a 12-bit, 1MSPS successive-approximation analog-to-digital converter with an on-chip sample-and-hold amplifier and voltage reference.

The IP feature nine analog input channels (1 channel can be set as voltage divider input) with an inside temperature sensor channel, totally 10-channels. Input multiplex are built inside that allow a preprogrammed selection of channels to be converted.

The IP has internal AVDD reference and external reference selection. An external reference can be chosen to let the users can select a variety of input ranges.

A single clock input is used to control all internal conversion cycles. The digital output data is presented in straight binary format.

4.2. Features

- Internal AVDD reference / External Reference Option
- 10 input channels with input-mux
- AIN0~AIN7 for outside PINs
- AIN8 for outside PIN with voltage divider option
- IN9 is internal temperature sensor
- Throughout Rate: ≤ 1 MHz
- DNL: ± 1 LSB
- INL: ± 2 LSB
- Active Area : TBD
- Power Consumption: ≤ 700 uA
- Power-Down Mode
- Straight Binary Output Format

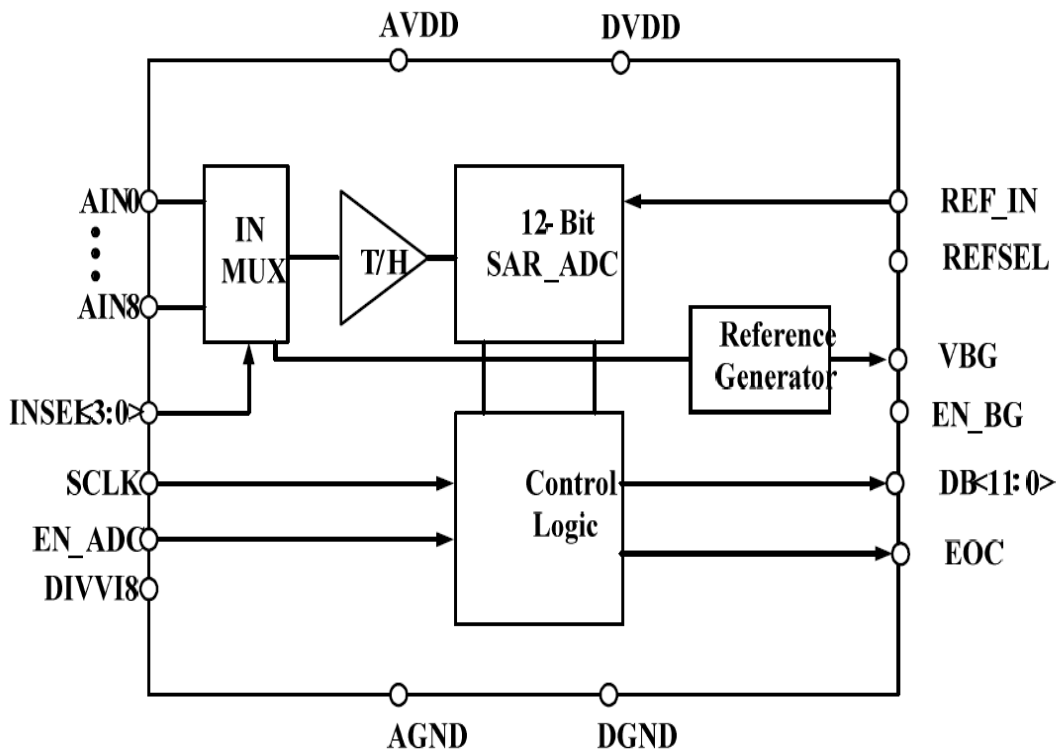


Figure 4-1 Analog-to-Digital Converters (ADC) Architecture

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5. FPGA Architecture

5.1. Functional Description

The programmable logic of AGM PSoC contain an industrial state-of-the art two-dimensional row- and column-based architecture to implement custom logic. Column and row interconnects of varies speeds provide signal interconnects between logic blocks (LBs) and IOs.

The logic array consists of LBs, with 16 logic slices (LS) in each LB. A slice is a small unit of logic providing efficient implementation of user logic functions. LBs are grouped into rows and columns across the device.

The device global clock network consists of up to 10 global clock lines that drive through the entire device. The global clock network can provide clocks for all resources within the device, such as input/output elements (IOEs), slices. The global clock lines can also be used for other high fan-out signals.

Each device I/O pin is fed by an IOE located at the ends of LB rows and columns around the periphery of the device. I/O pins support various single-ended standards. Each IOE contains a bidirectional I/O buffer.

5.2. Logic Array Blocks

Each Logic Block consists of 16 slices, SLICE carry chains, SLICE control signals, a local interconnect, a look-up table (LUT) chain, and register chain connection lines. There are 32 possible unique inputs into an SLICE. Register chain connections transfer the output of one SLICE's register to the adjacent SLICE's register within a block. The AG software places asPSoCiated logic within an SLICE or adjacent SLICES, allowing the use of local, LUT chain, and register chain connections for performance and area efficiency.

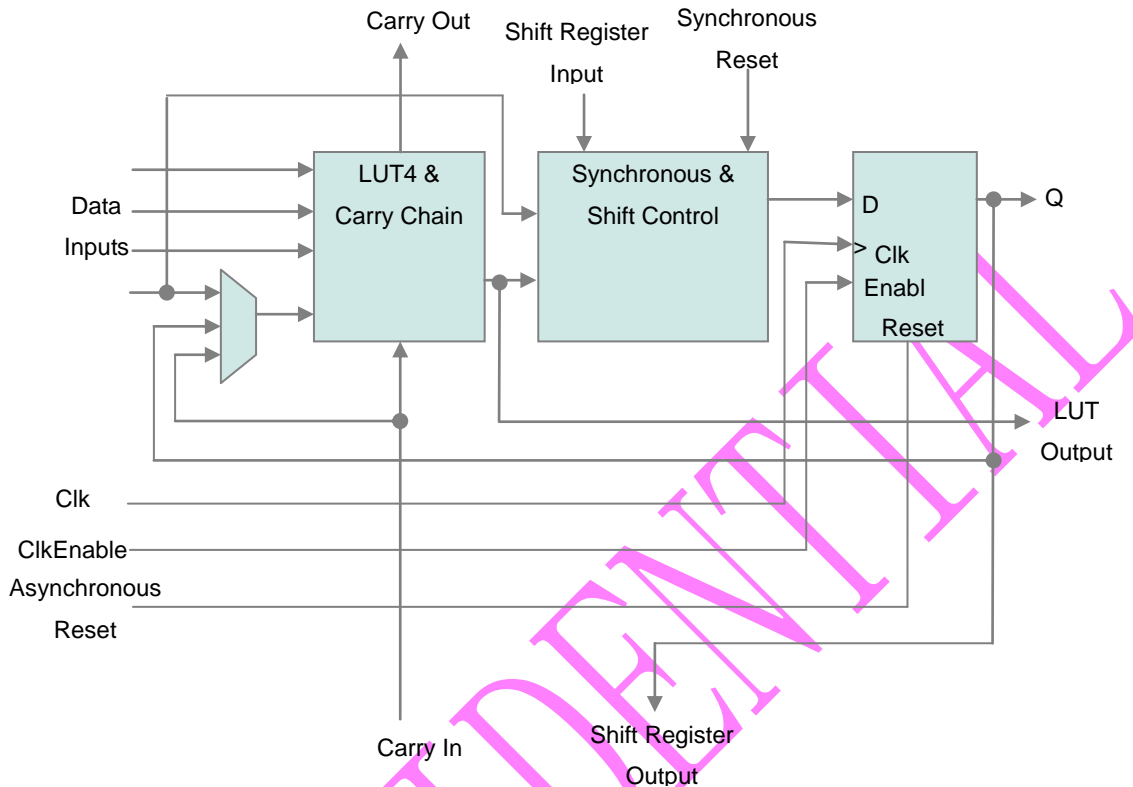
5.3. Logic Element

The smallest unit of logic in AGM FPGA architecture, the slice, is compact and provides advanced and flexible features with efficient logic utilization. Each slice features:

- Industrial standard four-input look-up table (LUT4), which is a function generator that can implement any combinatorial logic function of four inputs.
- A programmable register
- A carry chain connection
- A register chain connection
- The ability to drive all types of interconnects: local, row, column, register chain, and inter-tile connections
- Support for efficient packing of LUT and register

- Support for register feedback

Figure 6-1. AGM FPGA Logic SLICE



Each slice's register has data, clock, clock enable, and clear inputs. Signals that from global clock network, general-purpose I/O pins, or any internal logic outputs can drive the register's clock and clear control signals. Either general-purpose I/O pins or internal logic can drive the clock enable. For combinational functions, the LUT output bypasses the register and drives directly to the slice outputs resources. The slice is architected so that LUT and register can drive to separate outputs.

5.4. FlexTrack Interconnect

In FPGA architecture of AGM PSoC, FlexTrack interconnect consists of continuous, performance-optimized routing lines used for inter- and intra- design block connectivity. The FlexTrack connects to LEs, and IO pins with row and column connection that span fixed distances.

5.5. Clock Networks

The AGM PSoC device support 15 dedicated clock pins that can drive 20 global clocks (GCLKs). GCLKs drive throughout the entire device, feeding all device quadrants. All resources in the device (I/O elements, logic array blocks (LABs), dedicated multiplier blocks, and M9K memory blocks) can use

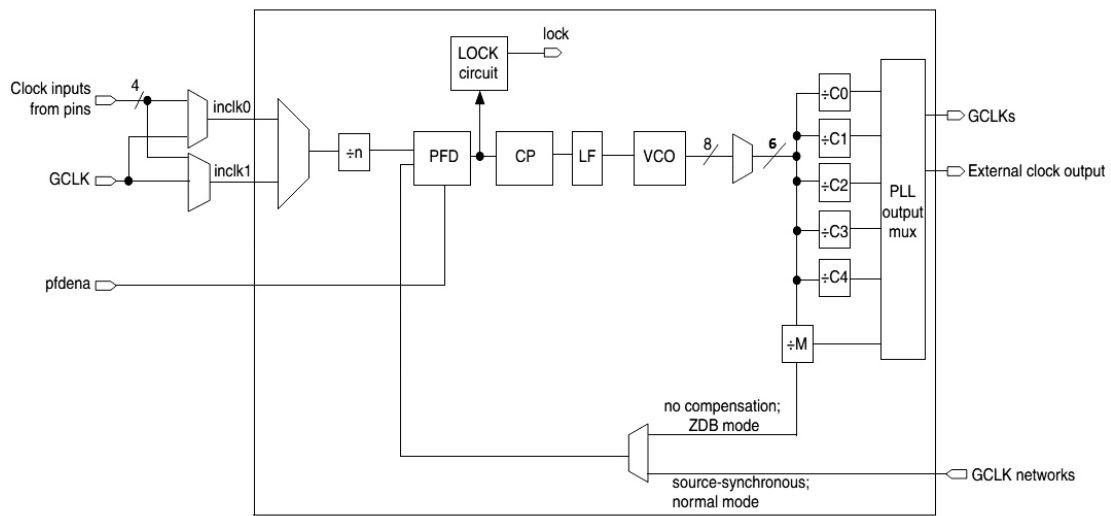
GCLKs as clock sources. Use these clock network resources for control signals, such as clock enables and clears fed by an external pin. Internal logic can also drive GCLKs for internally generated GCLKs and asynchronous clears, clock enables, or other control signals with high fan-out.

5.6. Phase Locked Loops (PLLs)

The FPGA architecture of AGM PSoC devices contain 4 general purpose PLLs that provide robust clock management and synthesis for device clock management, external system clock management, and high-speed I/O interfaces.

Figure 6-2 shows a block diagram of the major components of the PLL of AGM PSoC FPGA architecture.

Figure 6-2. AGM FPGA PLL Block Diagram



Each clock source can come from any of the clock pins located on the same side of the device as the PLL. The general I/O pins cannot drive the PLL clock input pins.

AGM FPGA PLLs support four different clock feedback modes. Each mode allows clock multiplication and division, phase shifting, and programmable duty cycle. For the supported feedback modes and other features, refer to Table 6.1.

Table 6-1. AGM PSoC FPGA PLL Features

Hardware Features	Availability
Compensation modes	Source-Synchronous Mode, No Compensation Mode, Normal Mode, Zero Delay Buffer Mode
C (output counters)	5
M, N, C counter sizes	1 to 512
Dedicated clock outputs	1 single-ended or 1 differential pair
Clock input pins	4 single-ended or 2 differential pairs
Spread-spectrum input clock	Support

tracking	
PLL cascading	Through GCLK
Phase shift resolution	Down to 96-ps increments
Programmable duty cycle	Support
Output counter cascading	Support
Loss of lock detection	Support

5.7.Embedded Block RAM

The AGM PSoC FPGA contains up to 504 Kbits Embedded Block RAMs (EBRs). The embedded memory structure consists of columns of M9K memory blocks that you can configure to provide various memory functions, such as RAM, shift registers, ROM, and FIFO buffers.

M9K blocks support the following features:

- 8,192 memory bits per block (9,216 bits per block including parity)
- Independent read-enable (rden) and write-enable (wren) signals for each port
- Packed mode in which the M9K memory block is split into two 4.5 K single-port RAMs
- Variable port configurations
- Single-port and simple dual-port modes support for all port widths
- True dual-port (one read and one write, two reads, or two writes) operation
- Byte enables for data input masking during writes
- Two clock-enable control signals for each port (port A and port B)
- Initialization file to pre-load memory content in RAM and ROM modes

Table 6-2. lists the features supported by the M9K memory.

Table 6-2. Summary of M9K Memory Features

Feature	M9K Blocks
Configurations (depth x width)	8192 x 1
	4096 x 2
	2048 x 4
	1024 x 8
	1024 x 9
	512 x 16
	512 x 18
	256 x 32
	256 x 36
Parity bits	Support
Byte enable	Support
Packed mode	Support
Address clock enable	Support
Single-port mode	Support
Simple dual-port mode	Support

True dual-port mode	Support
Embedded shift register mode	Support
ROM mode	Support
FIFO buffer	Support
Simple dual-port mixed width support	Support
True dual-port mixed width support	Support
Memory initialization file	Support
Mixed-clock mode	Support
Power-up condition	Outputs cleared
Register asynchronous clears	Read address registers and output registers only
Latch asynchronous clears	Output latches only
Write or read operation triggering	Write and read: Rising clock edges
Same-port read-during-write	Outputs set to Old Data or New Data
Mixed-port read-during-write	Outputs set to Old Data or Don't Care

AGM PSoC FPGA devices M9K memory blocks allow you to implement fully-synchronous SRAM memory in multiple modes of operation. M9K memory blocks do not support asynchronous (unregistered) memory inputs. M9K memory blocks support the following modes:

Single-port, Simple dual-port, True dual-port, Shift-register, ROM, FIFO

5.8. Embedded Multipliers

AGM PSoC FPGA devices include a combination of on-chip resources that help increase performance, reduce system cost, and lower the power consumption of digital signal processing (DSP) systems. AGM PSoC FPGA devices, either alone or as DSP device co-processors, are used to improve price-to-performance ratios of DSP systems. Particular focus is placed on optimizing AGM PSoC FPGA devices for applications that benefit from an abundance of parallel processing resources, which include video and image processing, wireless communications, and multi-channel communications and video systems.

The embedded multiplier is configured as either one 18 × 18 multiplier or two 9 × 9 multipliers. For multiplications greater than 18 × 18, the AGM software cascades multiple embedded multiplier blocks together. There are no restrictions on the data width of the multiplier, but the greater the data width, the slower the multiplication process.

You can use an embedded multiplier block in one of two operational modes, depending on the application needs:

- One 18 × 18 multiplier
- Up to two 9 × 9 independent multipliers

You can also use embedded multipliers of AGM PSoC FPGA devices to implement multiplier adder and multiplier accumulator functions, in which the multiplier portion of the function is implemented with embedded multipliers, and the adder or accumulator function is implemented in logic elements (LEs).

5.9. I/O

AGM PSoC FPGA architecture support these I/O features:

- Supports 3.3-V, 2.5-V, 1.8-V, and 1.5-V logic levels: LVTTTL, LVCMOS
- Programmable drive strength, bus-hold, pull-up resistors, open-drain output, input and output delay, slew rate control.
- Differential I/O standards: LVPECL, True-LVDS, RSDS, Mini-LVDS, BLVDS.

I/O pins on AGM PSoC FPGA devices are grouped together into I/O banks. Each bank has a separate power bus. AGM PSoC FPGA devices have eight I/O banks. Each device I/O pin is associated with one I/O bank. All single-ended and differential I/O standards are supported in all banks. All differential I/O standards are supported in all banks.

AGM PSoC FPGA devices can send and receive data through LVDS signals. For the LVDS transmitter and receiver, the input and output pins of devices support serialization and deserialization through internal logic.

The BLVDS extends the benefits of LVDS to multipoint applications such as bidirectional backplanes. The loading effect and the need to terminate the bus at both ends for multipoint applications require BLVDS to drive out a higher current than LVDS to produce a comparable voltage swing. All the I/O banks support BLVDS for user I/O pins.

The RSDS and mini-LVDS standards are derivatives of the LVDS standard. The RSDS and mini-LVDS I/O standards are similar in electrical characteristics to LVDS, but have a smaller voltage swing and therefore provide increased power benefits and reduced electromagnetic interference (EMI).

The LVDS standard does not require an input reference voltage, but it does require a 100-ohm termination resistor between the two signals at the input buffer. An external resistor network is required on the transmitter side for the top and bottom I/O banks.

5.10. External Memory Interfaces

AGM PSoC FPGA architecture can easily interface with a broad range of external memory devices, including DDR2 SDRAM, DDR SDRAM, and QDR II SRAM. External memory devices are an important system component of a wide range of image processing, storage, communications, and general embedded applications.

AG16K PSoC FPGA devices use data (DQ), data strobe (DQS), clock, command, and address pins to interface with external memory.

6. Device Configuration

6.1. Configuration Flow

AGM PSoC device store the configuration data in the SPI flash. The stored configuration files contain MCU configuration file and FPGA configuration file. After the device power is up, the FPGA configuration file is loaded first and then MCU init configuration logic load MCU configuration file from the specified address of the internal SPI flash.

6.2. Configuration Data Compression

AGM FPGA configuration file support configuration data decompression, which saves configuration memory space and time. This feature allows you to store compressed configuration data in configuration devices or other memory and send the compressed bitstream to AGM FPGA devices. During configuration, AGM FPGA devices decompress the bitstream in real time and program the SRAM cells. When you enable compression, the AGM software generates configuration files with compressed configuration data. This compressed file reduces the storage requirements in the configuration device or flash memory and decreases the time required to send the bitstream to the AGM FPGA device.

7. DC Electrical Characteristics

7.1. Power-On Reset Circuitry

When power is applied to AGM PSoC devices, the POR circuit monitors V_{CC} and begins SRAM download at an approximate voltage of 1.2V AGM PSoC devices.

Entry into user mode is gated by whether V_{CCIO} bank are powered with sufficient operating voltage. If V_{CC} and V_{CCIO} are powered simultaneously, the device enters user mode.

For AGM PSoC when in user mode, the POR circuitry continues to monitor the V_{CC} (but not V_{CCIO}) voltage level to detect a brown-out condition. If there is a V_{CC} voltage sag at during user mode, the POR circuit resets the SRAM and tri-states the I/O pins. Once V_{CC} rises back to approximately 1.2V, the SRAM download restarts and the device begins to operate.

The below tables are the AGM PSoC power electrical characteristics.

Table 8-1 Absolute Maximum Ratings for AGM FPGA Devices

Symbol	Parameter	Min	Max	Unit
VCCINT	Core voltage	-0.5	1.8	V
VCCA	Phase-locked loop (PLL) analog power supply	-0.5	3.75	V
VCCD_PLL	PLL digital power supply	-0.5	4.5	V
VCCIO	I/O banks power supply	-0.5	3.75	V
VCC_CLKIN	Differential clock input pins power supply	-0.5	4.5	V
VI	DC input voltage	-0.5	4.2	V
IOUT	DC output current, per pin	-25	40	mA
TSTG	Storage temperature	-65	150	°C
TJ	Operating junction temperature	-40	100	°C

Table 8-2. Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VCCINT	Supply voltage for internal logic, 1.2V operation	-	1.15	1.2	1.25	V
VCCIO	Supply voltage for output buffers, 3.3-V operation	-	3.135	3.3	3.465	V
	Supply voltage for output buffers, 2.5-V operation	-	2.375	2.5	2.625	V
	Supply voltage for output buffers, 1.8-V operation	-	1.71	1.8	1.89	V
	Supply voltage for output buffers, 1.5-V operation	-	1.425	1.5	1.575	V

VCCA	Supply (analog) voltage for PLL regulator	-	2.375	2.5	2.625	V
VCCD_PLL	Supply (digital) voltage for PLL, 1.2-V operation	-	1.15	1.2	1.25	V
Vi	Input voltage	-	-0.5	-	3.6	V
Vo	Output voltage	-	0	-	VCCI O	V
Tj	Operating junction temperature	For commercial use	0	-	85	°C
		For industrial use	-40	-	100	°C
tRAMP	Power supply ramp time	Standard power-on reset (POR)	50 μ s	-	50 ms	-
		Fast POR	50 μ s	-	3 ms	-

Table 8-3. I/O Pin Leakage Current

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Ii	Input pin leakage current	Vi = 0 V to VCCIOMAX	-10	-	10	μ A
Ioz	Tristated I/O pin leakage current	Vo = 0 V to VCCIOMAX	-10	-	10	μ A

Table 8-4. Single-Ended I/O Standard Specifications

I/O Standard	VCCIO (V)			VIL (V)		VIH (V)		VoL (V)	VoH (V)	IoL (mA)	IoH (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
3.3-V LVTTTL	3.135	3.3	3.465	-	0.8	1.7	3.6	0.45	2.4	4	-4
3.3-V LVCMOS	3.135	3.3	3.465	-	0.8	1.7	3.6	0.2	VCCIO -0.2	2	-2
2.5 V	2.375	2.5	2.625	-0.3	0.7	1.7	VCCIO +0.3	0.4	2.0	1	-1
1.8 V	1.71	1.8	1.89	-0.3	0.35 x VCCIO	0.65 x VCCIO	2.25	0.45	VCCIO -0.45	2	-2
1.5 V	1.425	1.5	1.575	-0.3	0.35 x VCCIO	0.65 x VCCIO	VCCIO +0.3	0.25 x VCCIO	0.75 x VCCIO	2	-2

Table 8-5. Differential I/O Standard Specifications

I/O Standard	V _{CCIO} (V)			V _{ID} (mV)		V _{ICM} (V)		
	Min	Typ	Max	Min	Max	Min	Condition	Max
LVPECL	2.375	2.5	2.625	100	-	0.05	D _{MAX} ≤ 500 Mbps	1.80
						0.55	500 Mbps ≤ D _{MAX} ≤ 700 Mbps	1.80
						1.05	D _{MAX} > 700 Mbps	1.55
LVDS	2.375	2.5	2.625	100	-	0.05	D _{MAX} ≤ 500 Mbps	1.80
						0.55	500 Mbps ≤ D _{MAX} ≤ 700 Mbps	1.80
						1.05	D _{MAX} > 700 Mbps	1.55

I/O Standard	V _{CCIO} (V)			V _{ID} (mV)		V _{OD} (mV)			V _{OS} (V)		
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max
LVDS	2.375	2.5	2.625	100	-	247	-	600	1.125	1.25	1.375
BLVDS	2.375	2.5	2.625	100	-	-	-	-	-	-	-
mini-LVDS	2.375	2.5	2.625	-	-	300	-	600	1.0	1.2	1.4
RSDS	2.375	2.5	2.625	-	-	100	200	600	0.5	1.2	1.5

8. System Address & Registers for MCU

The comprehensive system level address map and MCU registers is shown in doc "Manual_MCU_M3_AG16K".

9. Pin-Outs

Refer to Pin-Outs printouts for AGM PSoC device family.

10. Software

AGM Software tools support from RTL to bit stream configuration implementation and programming. Supported operating system platforms include Microsoft Windows and Linux.

11. Ordering Information

Table11-1 Device Part Number Description

AG16K XX X XXX X

Optional:
G = GND Pad needed

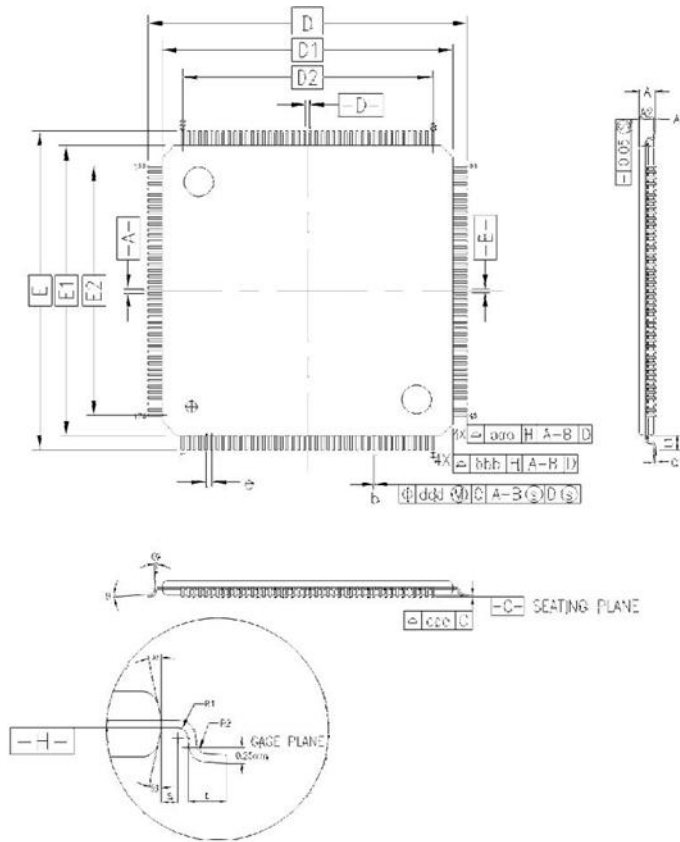
Pin Count:
176, 256

Package Type:
E = EQFP
F = FBGA (1 mm Pitch)

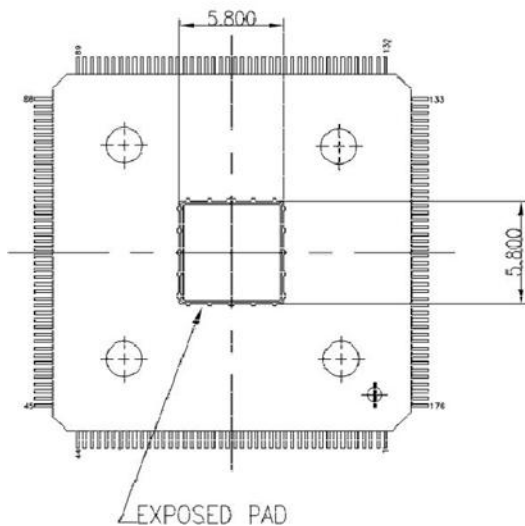
SD = SDRAM Embedded
DD = DDR RAM Embedded
Blank = FPGA Only

12. Package

EQFP-176



PKG. BOTTOM SIDE

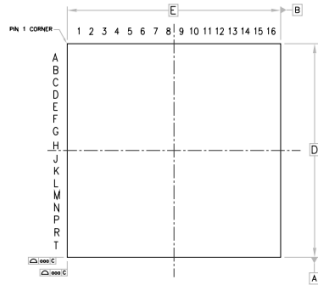


CONTROL DIMENSIONS ARE IN MILLIMETERS.

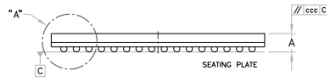
SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.00	1.10	1.20	0.039	0.043	0.047
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.05	1.00	1.05	0.002	0.039	0.041
D	22.00	BSC.		0.866	BSC.	
D1	20.00	BSC.		0.787	BSC.	
E	22.00	BSC.		0.866	BSC.	
E1	20.00	BSC.		0.787	BSC.	
R2	0.08	—	0.20	0.003	—	0.008
R1	0.08	—	—	0.003	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ ₁	0°	—	—	0°	—	—
θ ₂	11°	12°	13°	11°	12°	13°
θ ₃	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
l	0.45	0.60	0.75	0.018	0.024	0.030
L ₁	1.00 REF.			0.039 REF.		
S	0.20	—	—	0.008	—	—

SYMBOL	176L					
	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
b	0.13	0.16	0.23	0.005	0.006	0.009
e	0.40 BSC.			0.016 BSC.		
D2	17.20			0.677		
E2	17.20			0.677		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.07			0.003		

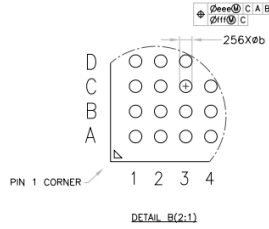
FBGA-256



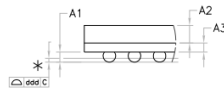
TOP VIEW



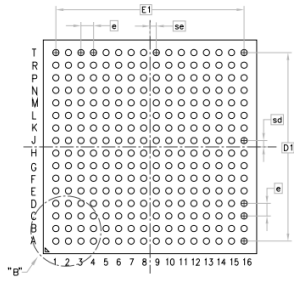
SIDE VIEW



DETAIL B(2:1)



DETAIL A(2:1)



BOTTOM VIEW

FOR CUSTOMER ONLY		LFBGA		
PACKAGE TYPE		256		
PIN COUNT		256		
DESCRIPTION	SYMBOL	MILLIMETER		
		MIN	NOM	MAX
TOTAL THICKNESS	A	-	1.46	1.55
STAND OFF	A1	0.35	0.40	0.45
MOLD THICKNESS	A2	-	0.70 _{BSC}	-
MATERIAL THICKNESS	A3	0.32	0.36	0.40
PACKAGE SIZE	D	16.90	17.00	17.10
	E	16.90	17.00	17.10
BALL PITCH	e	-	1.00 _{BSC}	-
BALL SIZE	b	0.45	0.50	0.55
EDGE BALL CENTER TO CENTER	D1	-	15.00 _{BSC}	-
EDGE BALL CENTER TO CENTER	E1	-	15.00 _{BSC}	-
PACKAGE EDGE PROFILE	aaa	-	0.10	-
SUBSTRATE FLATNESS	bbb	-	-	-
MOLD FLATNESS	ccc	-	0.10	-
BALL COPLANARITY	ddd	-	0.15	-
BALL POSITION OFFSET (PACKAGE)	eee	-	0.15	-
BALL POSITION OFFSET (BALL)	fff	-	0.08	-
	sd	-	0.50	-
	se	-	0.50	-

CONFIDENTIAL

13.Recommended Reflow Profile

Figure. 13-1 Classification Reflow Profile

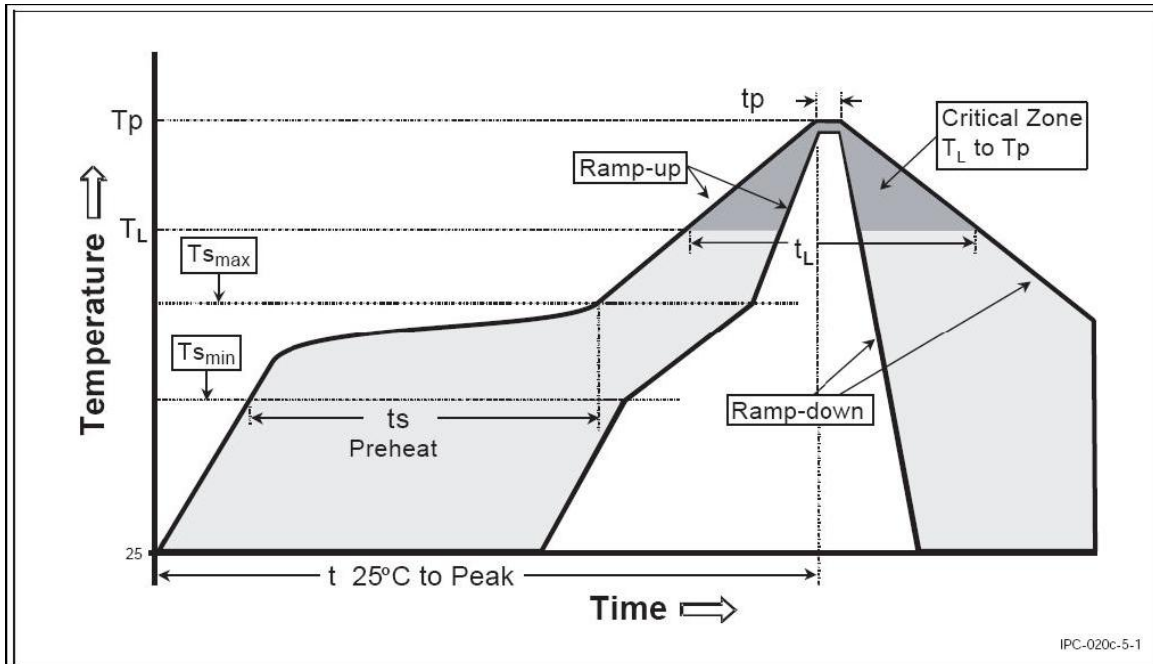


Table 13-1 Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average Ramp-Up Rate (T _{Smax} to T _p)	3 °C/second max.	3 °C/second max.
Preheat		
-Temperature Min (T _{Smin})	100 °C	150 °C
-Temperature Max (T _{Smax})	100 °C	200 °C
-Time (t _{Smin} to t _{Smax})	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (T _L)	183 °C	217 °C
-Time (t _L)	60-150seconds	60-150 seconds
Peak /Classification Temperature(T _p)	See Table 10	See Table 11
Time within 5 oC of actual Peak Temperature (t _p)	10-30 seconds	20-40 seconds
Ramp-Down Rate	6 °C/second max.	6 °C/seconds max.
Time 25 oC to Peak Temperature	6 minutes max.	8 minutes max.

Table 13-2 Sn-Pb Eutectic Process – Package Peak Reflow Temperatures

Package Thickness	Volume mm3 <350	Volume mm3 ≥350
<2.5mm	240 + 0/-5 °C	225 + 0/-5 °C
≥2.5mm	225 + 0/-5 °C	225 + 0/-5 °C

Table 13-3 Pb-free Process – Package Classification Reflow Temperatures

Package Thickness	Volume mm3 <350	Volume mm3 350-2000	Volume mm3 >2000
<1.6mm	260 + 0 °C *	260 + 0 °C *	260 + 0 °C *
1.6mm – 2.5mm	260 + 0 °C *	250 + 0 °C *	245 + 0 °C *
≥2.5mm	250 + 0 °C *	245 + 0 °C *	245 + 0 °C *

*Tolerance : The device manufacturer/supplier shall assure process compatibility up to and including the stated classification temperature(this mean Peak reflow temperature + 0 °C. For example 260+ 0 °C) at the rated MSL Level.

- Note 1: All temperature refer topside of the package. Measured on the package body surface.
- Note 2: The profiling tolerance is + 0 °C, - X °C (based on machine variation capability)whatever is required to control the profile process but at no time will it exceed – 5 °C. The producer assures process compatibility at the peak reflow profile temperatures defined in Table 9-3.
- Note 3: Package volume excludes external terminals(balls, bumps, lands, leads) and/or non integral heat sinks.
- Note 4: The maximum component temperature reached during reflow depends on package the thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD package may sill exist.
- Note 5: Components intended for use in a “lead-free” assembly process shall be evaluated using the “lead free” classification temperatures and profiles defined in Table8-1, 8-2, 8-3 whether or not lead free.

14. Change List

The following table summarizes revisions to this document.

REV	DATE	AUTHER	CHANGE DESCRIPTION
V1.0	02/11/2018		Release Version 1.0

15. RoHS Compliant

The product does not contain lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB) or polybrominated diphenyl ethers (PBDE), and are therefore considered RoHS compliant.

16. ESD Precautions

ESD protection circuitry is contended in this device, but special handling precautions are required.