DATA SHEET

Revision: 1.0

AGM AG6K SoC

Low Cost and High Integration SoC

General Description

AGM AG6K SoC is targeted to high-volume, cost-sensitive, applications, enabling system designers to meet increasing performance requirements while lowering costs. It is based on AGM SoC architecture

This device integrate one ARM® Cortex™ core, AGM programmable logic, 12-bit ADC, 64Mbits SDRAM and 12Mbits SPI NOR FLASH in single device.

The AGM SoC, its low cost and optimized feature set makes ideal solutions for a wide array of consumer, communications, video processing, test and measurement, and other end-market solutions.

Features

MCU Architecture:

• **One-core ARM® Cortex™:** Working frequency up to 250 MHz

• **On-Chip Memory:** 128Kbytes SRAM

• **I/O Interfaces:**

- External AHB Slave Interface
- On-Chip Memory Access Ports
- UART Interface
- GPIOs
- JTAG Debug Ports
- SPI Flash Interface

• **Interconnect:** ARM AMBA® AHB based

SDRAM:

- 16bits datawidth
- 64Mbits capability
- up to 166MHz working frequency

SPI Flash:

- 12Mbits capability

Analog-to-Digital Converters（ADC）：

- 12bits accuracy
- 1MHz sampling frequency
- On-chip temperature sensing
- Up to 10 channels(include internal temperature sensor channel)

FPGA Architecture:

- High-density architecture with 6K LEs
- M9K embedded memory blocks, up to 504 Kbits of RAM space
- Up to 56 18 x 18-bit embedded multipliers are each configurable as two independent 9 x 9-bit multipliers
- Provides 4 PLLs per device provide clock multiplication and phase shifting
- High-speed differential I/O standard support, including LVDS, RSDS, mini-LVDS, LVPECL
- support DDR, DDR2
- Single-ended I/O standard support, including 3.3V, 2.5V, 1.8V, and 1.5V LVCMOS and LVTTL
- Flexible device configuration mode: JTAG and AS, PS
- Support remote update, by "dual-boot" like implementation

•

Contents

1. Feature Summary

Table 1-1: AGM SoC

AGM SoC		
Device Name		**AG6KMCUSoC**
MCU	**Processor Core**	ARM Cortex
	Maximum Frequency	250MHz
	On-Chip Memory(SRAM)	128KBytes
	Interfaces	AHB Slave Interface, On-Chip Memory Acess Port, 1 x UART, 24 x GPIOs, 1 x SPI Flash Interface
SDRAM	**Capability**	64M bits
	Datawidth	16 bits
	Max Working Frequency	133MHz
FLASH	**Capability**	12M bits
ADC	**Sampling accuracy**	12bits
	Sampling frequency	1MHz
	Max input channels	Up to 10 channels(include on-chip temperature sensor channel)
FPGA	**Logic elements (LEs)**	6272
	Embedded memory (Kbits)	504
	Embedded 18 × 18 multipliers	56
	General-purpose PLLs	2
	Global Clock Networks	10
	User I/O Banks	8

Table 1-2: Device-Package Combinations: Maximum I/Os

Device	AG6KMCUSoC
Package	LQFP100
Body Size(mm)	16 x 16
Pitch(mm)	0.8
Max User IO	66

Figure 1-1 illustrates the functional blocks of AGM SoC.

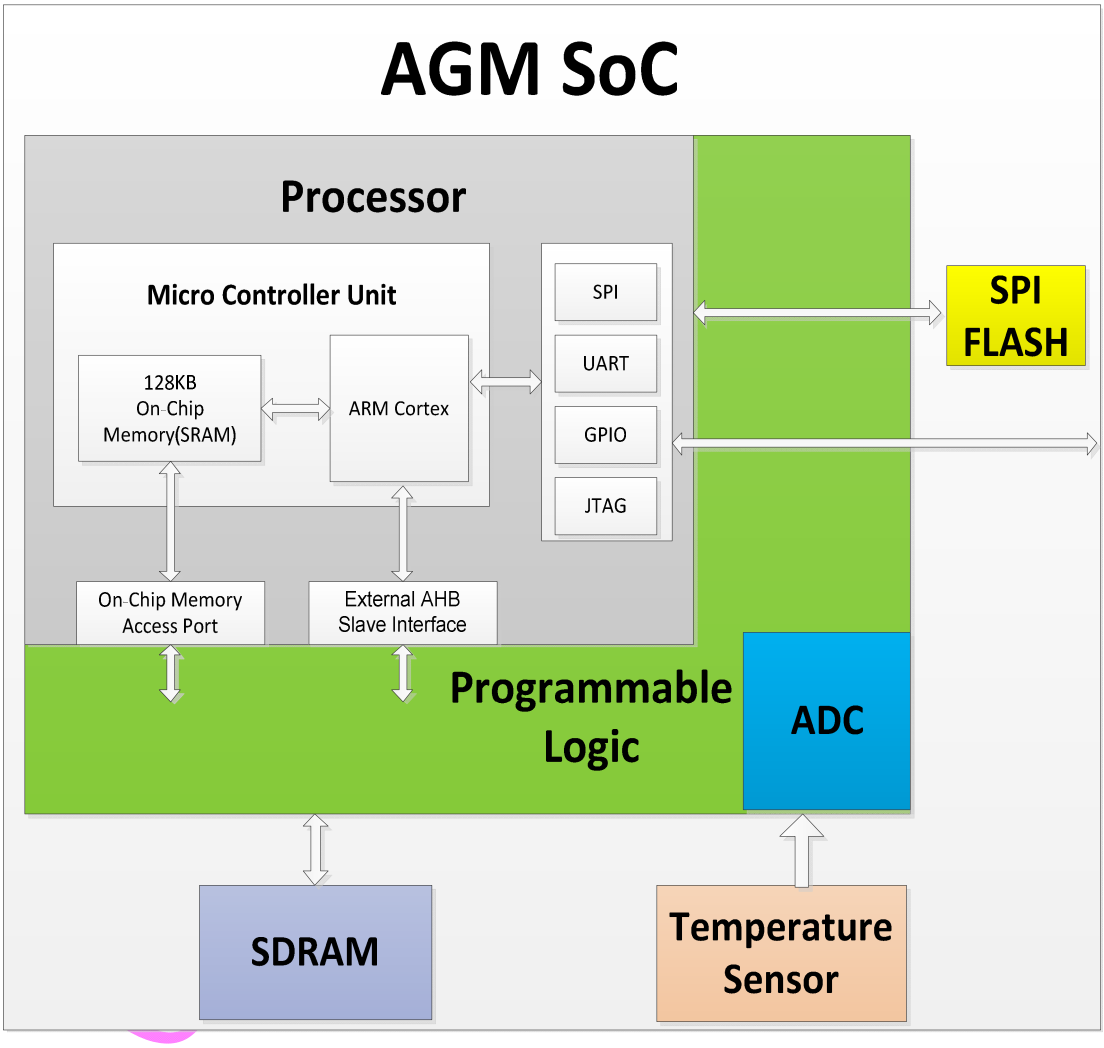


Figure 1: AGM SoC Overview

2. MCU Architecture

2.1. Functional Description

The AGM SoC device contains an processor, a FPGA, a SDRAM, an ADC and a Flash in one chip with laminated seal technology.

The AGM SoC offers the flexibility and scalability of an FPGA, while providing performance, power, and ease of use typically associated with ASIC and ASSPs.

As shown in Figure 1-1, the MCU comprises four major blocks:

- Processor Unit
- On-Chip Memory Access Interface
- External AHB Slave Interface
- I/O peripherals (IOP)

2.2. Processor Unit

The key features of the Processor Unit include:

- 32-bit Micro Processor
- Maximum Frequency: 250MHz
- On-Chip Memory(SRAM): 128Kbytes
- Single cycle multiplication and hardware division
- Integrated nested interrupt controller (NVIC)
- Two timers(each timer can be configured as a 32 bit timer or two 16 bit timers)
- Private Watch Dog timer
- Cortex M3 embedded tracking module (ETM)
- Serial Debug mode (SWP)

2.3. On-Chip Memory Access Interface

The on-chip memory module contains 128 KB of RAM. It is accessed by Micro Processor and programmable logic through AHB bus interconnect.

On-chip memory supports high read and write throughput for RAM access by implementing the RAM as a four-byte memory (32 bits).

Table 2-1 introduces the On-Chip memory access interface port function.

Table 2-1 On-Chip Memory Access Ports

Pin Name	I/O Direction	Function
EXT_RAM_EN	Input	RAM enable, active high
EXT_RAM_WR	Input	RAM write/read control, write — 1 read — 0
EXT_RAM_ADDR[13:0]	Input	RAM address
EXT_RAM_BYTE_EN [3:0]	Input	RAM data byte enable, active high
EXT_RAM_WDATA[31:0]	Input	RAM write data
EXT_RAM_RDATA[31:0]	Output	RAM read data

2.4. External AHB Slave Interface

The MCU provide another external AHB slave interface for FPGA data communication like as On-Chip memory access interface. The AHB slave interface can support 32-bit write and read data interface for FPGA.

Table 2-2 introduces the external AHB slave ports function.

Table 2-2 External AHB Slave Ports

Pin Name	I/O Direction	Function
HRESP_EXT[1:0]	Input	--
HREADY_OUT_EXT	Input	FPGA Slave Ready
HRDATA_EXT[31:0]	Input	FPGA send data to MCU
HTRANS_EXT[1:0]	Output	--
HADDR_EXT[31:0]	Output	MCU access address
HWRITE_EXT	Output	Write Enable
HSEL_EXT	Output	--
HWDATA_EXT[31:0]	Output	MCU write data to FPGA
HSIZE_EXT[2:0]	Output	--
HREADY_IN_EXT	Output	--

2.5. I/O peripherals (IOP)

UART Port

The UART controller is a full-duplex asynchronous receiver and transmitter that supports a wide range of programmable baud rates and I/O signal formats. The controller can accommodate automatic parity generation and multi-master detection mode. The controller is structured with separate Rx and Tx data paths.

The UART controller has the following features:

- Programmable baud rate generator
- 64-byte receive and transmit FIFOs
- Programmable protocol:
- 6, 7, or 8 data bits
- 1, 1.5, or 2 stop bits
- Odd, even, space, mark, or no parity
- Parity, framing and overrun error detection
- Line-break generation
- Interrupts generation
- RxD and TxD modes: Normal/echo and diagnostic loopbacks using the mode switch

Table 2-3 introduces the UART ports function.

Table 2-3 UART Ports

Pin Name	I/O Direction	Function
UART_RXD	Input	UART Receive Serial Data
UART_CTS_n	Input	Clear to Send
UART_TXD	Output	UART Send Serial Data
UART_RTS_n	Output	Require To Send

SPI Flash Interface

The MCU can use SPI flash interface to access the internal spi flash, or through FPGA I/O to access other external spi flash device.

The flash interface has following features :

- 4-bit parallel NOR flash supporting up to 64 MB
- ONFi 1.0 NAND flash support with 1-bit ECC
- 1-bit SPI, 2-bit SPI, 4-bit SPI (quad-SPI) serial NOR flash

Table 2-4 introduces the SPI flash ports function.

Table 2-4 SPI Flash Ports

Pin Name	I/O Direction	Function
FLASH_BIAS[23:0]	Input	Flash offset address
FLASH_SCK	Output	Flash access clock
FLASH_CS_n	Output	Flash chip select, active low
FLASH_IO0_SI	Output	MCU data to flash
FLASH_IO1_SO	Output	--
FLASH_IO2_WPn	Output	Flash write protection, active low

FLASH_IO3_HOLDn	Output	Flash hold signal, active low
FLASH_IO0_SI_i	Input	--
FLASH_IO1_SO_i	Input	Flash data to MCU
FLASH_IO2_WPn_i	Input	--
FLASH_IO3_HOLDn_i	Input	--
FLASH_SI_OE	Output	Data in enable, active high
FLASH_SO_OE	Output	Data out enable, active high
WPn_IO2_OE	Output	WP enable, active high
HOLDn_IO3_OE	Output	Hold enable, active high

GPIOs

The GPIOs have following features:

- Up to 24 GPIO signals for device pins routed through FPGA
- Outputs are 3-state capable

The function of each GPIO can be dynamically programmed on an individual or group basis.

Table 2-5 introduces the GPIO ports function.

Table 2-5 GPIO Ports

Pin Name	I/O Direction	Function
GPIO0_I[7:0]	Input	GPIO0 byte data input, nGPEN0 as bit enable
GPIO1_I[7:0]	Input	GPIO1 byte data input, nGPEN1 as bit enable
GPIO2_I[7:0]	Input	GPIO2 byte data input, nGPEN2 as bit enable
GPIO0_O[7:0]	Output	GPIO0 byte data output，nGPEN0 as bit input/output enable，High – GPIO0_I enable，low – GPIO0_O enable
GPIO1_O[7:0]	Output	GPIO1 byte data output，nGPEN1 as bit input/output enable，High – GPIO1_I enable，low – GPIO1_O enable
GPIO2_O[7:0]	Output	GPIO2 byte data output，

		nGPEN2 as bit input/output enable，High – GPIO2_I enable，low – GPIO2_O enable
nGPEN0[7:0]	Output	GPIO0 byte output enable
nGPEN1[7:0]	Output	GPIO1 byte output enable
nGPEN2[7:0]	Output	GPIO2 byte output enable
O_INI_IP	Output	Active high, MCU initial process is on going and user can't access MCU

JTAG Debug Port

This JTAG debug port can be used to debug MCU code through FPGA IO. User can use J-LINK to debug the application.

Table 2-6 introduces the JTAG port.

Table 2-6 JTAG Debug Ports

Pin Name	**I/O Direction**	**Function**
JTCK	Input	JTAG clock input
JTDI	Input	JTAG data input
JTMS	Input	JTAG mode input
JTDO	Output	JTAG data output

3. SDRAM

3.1. Functional Description

The integrated SDRAM is a high speed synchronous dynamic random access memory (SDRAM), organized as 1024K words × 4 banks × 16 bits(64Mbits). The SDRAM delivers a data bandwidth of up to 166M words per second.

Accesses to the SDRAM are burst oriented. Consecutive memory location in one page can be accessed at a burst length of 1, 2, 4, 8 or full page when a bank and row is selected by an ACTIVE command.

Column addresses are automatically generated by the SDRAM internal counter in burst operation. Random column read is also possible by providing its address at each clock cycle. The multiple bank nature enables interleaving among internal banks to hide the precharging time.

3.2. Features

- Up to 166MHz Clock Frequency
- Capability 64Mbits : 1024Kwords × 4 banks × 16bits organization
- Self Refresh Mode
- CAS Latency: 2 and 3
- Burst Length: 1, 2, 4, 8 and full page
- Sequential and Interleave Burst
- Burst Read, Single Write Mode
- Byte data controlled by DQM0-3
- Auto-precharge and Controlled Precharge

4. FLASH

4.1. Functional Description

The 12Mbits flash supports the standard Serial Peripheral Interface (SPI), and supports the Dual/Quad SPI: Serial Clock, Chip Select, Serial Data I/O0 (SI), I/O1 (SO), I/O2 (WP#), and I/O3 (HOLD#). The Dual I/O data is transferred with speed of 240Mbits/s and the Quad I/O & Quad output data is transferred with speed of 480Mbits/s.

4.2. Features

- 12M-bits Serial Flash

  - 1.5M-Byte Capability
  - 256 Bytes per programmable page

- Standard, Dual, Quad SPI

  - Standard SPI: SCLK, CS#, SI, SO, WP#, HOLD#
  - Dual SPI: SCLK, CS#, IO0, IO1, WP#, HOLD#
  - Quad SPI: SCLK, CS#, IO0, IO1, IO2, IO3

- Fast Program/Erase Speed

  - Page Program time: 0.6ms typical
  - Sector Erase time: 45ms typical
  - Block Erase time: 0.15/0.25s typical
  - Chip Erase time: 4s typical

- Flexible Architecture

  - Uniform Sector of 4K-Byte
  - Uniform Block of 32/64K-Byte

- High Speed Clock Frequency

  - 120MHz for fast read with 30PF load
  - Dual I/O Data transfer up to 240Mbits/s
  - Quad I/O Data transfer up to 480Mbits/s

- Minimum 100,000 Program/Erase Cycles

- Data retention

  - 20-year data retention typical

5. Analog-to-Digital Converters(ADC)

5.1. Functional Description

The Analog-to-Digital Converters(ADC) is a 12-bit, 1MSPS successive-approximation analog-to-digital converter with an on-chip sample-and-hold amplifier and voltage reference.

The IP feature nine analog input channels (1 channel can be set as voltage divider input) with an inside temperature sensor channel, totally 10-channelas. Input multiplex are built inside that allow a preprogrammed selection of channels to be converted.

The IP has internal AVDD reference and external reference selection. An external reference can be chosen to let the users can select a variety of input ranges.

A single clock input is used to control all internal conversion cycles. The digital output data is presented in straight binary format.

5.2. Features

- Internal AVDD reference / External Reference Option
- 10 input channels with input-mux
- AIN0~AIN7 for outside PINs
- AIN8 for outside PIN with voltage divider option
- IN9 is internal temperature sensor
- Throughout Rate: <=1MHz
- DNL: +/- 1LSB
- INL: +/- 2LSB
- Active Area : TBD
- Power Consumption: <=700uA
- Power-Down Mode
- Straight Binary Output Format

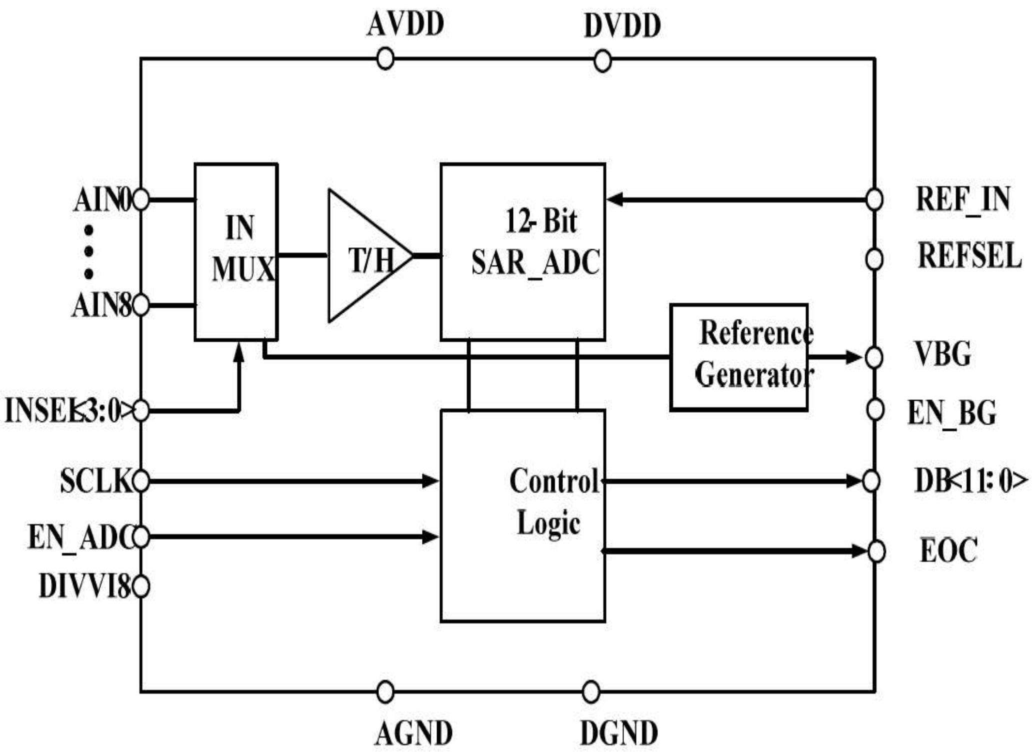


Figure 5-1 Analog-to-Digital Converters(ADC) Architecture

6. FPGA Architecture

6.1. Functional Description

The programmable logic of AGM SoC contain an industrial state-of-the art two-dimensional row- and column-based architecture to implement custom logic. Column and row interconnects of varies speeds provide signal interconnects between logic blocks (LBs) and IOs.

The logic array consists of LBs, with 16 logic slices (LS) in each LB. A slice is a small unit of logic providing efficient implementation of user logic functions. LBs are grouped into rows and columns across the device.

The device global clock network consists of up to 10 global clock lines that drive through the entire device. The global clock network can provide clocks for all resources within the device, such as input/output elements (IOEs), slices. The global clock lines can also be used for other high fan-out signals.

Each device I/O pin is fed by an IOE located at the ends of LB rows and columns around the periphery of the device. I/O pins support various single-ended standards. Each IOE contains a bidirectional I/O buffer.

6.2. Logic Array Blocks

Each Logic Block consists of 16 slices, SLICE carry chains, SLICE control signals, a local interconnect, a look-up table (LUT) chain, and register chain connection lines. There are 32 possible unique inputs into an SLICE. Register chain connections transfer the output of one SLICE's register to the adjacent SLICE's register within a block. The AG software places associated logic within an SLICE or adjacent SLICES, allowing the use of local, LUT chain, and register chain connections for performance and area efficiency.

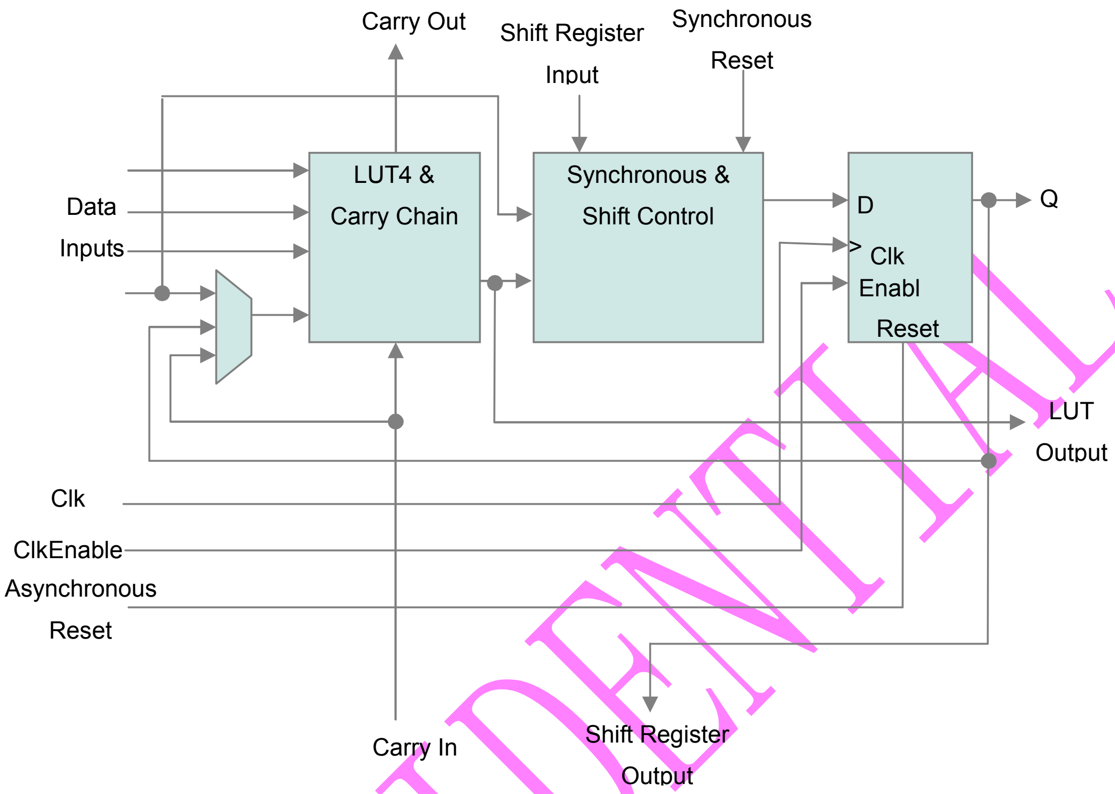
6.3. Logic Element

The smallest unit of logic in AGM FPGA architecture, the slice, is compact and provides advanced and flexible features with efficient logic utilization. Each slice features:

- Industrial standard four-input look-up table (LUT4), which is a function generator that can implement any combinatorial logic function of four inputs.
- A programmable register
- A carry chain connection
- A register chain connection
- The ability to drive all types of interconnects: local, row, column, register chain, and inter-tile connections
- Support for efficient packing of LUT and register

- Support for register feedback

Figure 6-1. AGM FPGA Logic SLICE



Each slice's register has data, clock, clock enable, and clear inputs. Signals that from global clock network, general-purpose I/O pins, or any internal logic outputs can drive the register's clock and clear control signals. Either general-purpose I/O pins or internal logic can drive the clock enable. For combinational functions, the LUT output bypasses the register and drives directly to the slice outputs resources. The slice is architected so that LUT and register can drive to separate outputs.

6.4. FlexTrack Interconnect

In FPGA architecture of AGM SoC, FlexTrack interconnect consists of continuous, performance-optimized routing lines used for inter- and intra- design block connectivity. The FlexTrack connects to LEs, and IO pins with row and column connection that span fixed distances.

6.5. Clock Networks

The AGM SoC device support 15 dedicated clock pins that can drive 20 global clocks (GCLKs). GCLKs drive throughout the entire device, feeding all device quadrants. All resources in the device (I/O elements, logic array blocks (LABs), dedicated multiplier blocks, and M9K memory blocks) can use

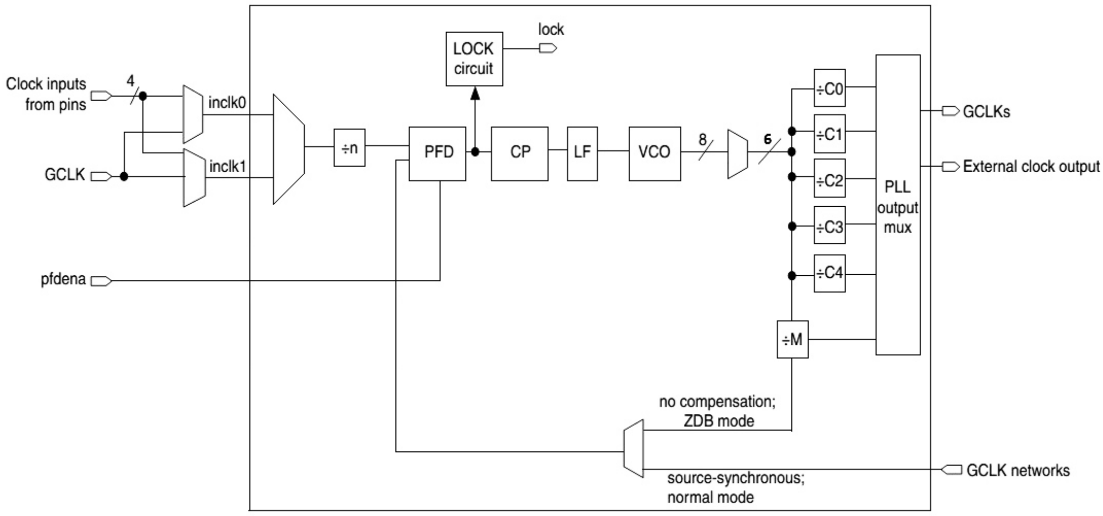
GCLKs as clock sources. Use these clock network resources for control signals, such as clock enables and clears fed by an external pin. Internal logic can also drive GCLKs for internally generated GCLKs and asynchronous clears, clock enables, or other control signals with high fan-out.

6.6. Phase Locked Loops (PLLs)

The FPGA architecture of AGM SoC devices contain 4 general purpose PLLs that provide robust clock management and synthesis for device clock management, external system clock management, and high-speed I/O interfaces.

Figure 6-2 shows a block diagram of the major components of the PLL of AGM SoC FPGA architecture.

Figure 6-2. AGM FPGA PLL Block Diagram



Each clock source can come from any of the clock pins located on the same side of the device as the PLL. The general I/O pins cannot drive the PLL clock input pins.

AGM FPGA PLLs support four different clock feedback modes. Each mode allows clock multiplication and division, phase shifting, and programmable duty cycle. For the supported feedback modes and other features, refer to Table 6.1.

Table 6-1. AGM SoC FPGA PLL Features

Hardware Features	Availability
Compensation modes	Source-Synchronous Mode, No Compensation Mode, Normal Mode, Zero Delay Buffer Mode
C (output counters)	5
M, N, C counter sizes	1 to 512
Dedicated clock outputs	1 single-ended or 1 differential pair

Clock input pins	4 single-ended or 2 differential pairs
Spread-spectrum input clock tracking	Support
PLL cascading	Through GCLK
Phase shift resolution	Down to 96-ps increments
Programmable duty cycle	Support
Output counter cascading	Support
Loss of lock detection	Support

6.7. Embedded Block RAM

The AGM SoC FPGA contains up to 504 Kbits Embedded Block RAMs (EBRs). The embedded memory structure consists of columns of M9K memory blocks that you can configure to provide various memory functions, such as RAM, shift registers, ROM, and FIFO buffers.

M9K blocks support the following features:

- 8,192 memory bits per block (9,216 bits per block including parity)
- Independent read-enable (rden) and write-enable (wren) signals for each port
- Packed mode in which the M9K memory block is split into two 4.5 K single-port RAMs
- Variable port configurations
- Single-port and simple dual-port modes support for all port widths
- True dual-port (one read and one write, two reads, or two writes) operation
- Byte enables for data input masking during writes
- Two clock-enable control signals for each port (port A and port B)
- Initialization file to pre-load memory content in RAM and ROM modes

Table 6-2. lists the features supported by the M9K memory.

Table 6-2. Summary of M9K Memory Features

Feature	M9K Blocks
Configurations (depth × width)	8192 × 1 4096 × 2 2048 × 4 1024 × 8 1024 × 9 512 × 16 512 × 18 256 × 32 256 × 36
Parity bits	Support
Byte enable	Support
Packed mode	Support
Address clock enable	Support

Single-port mode	Support
Simple dual-port mode	Support
True dual-port mode	Support
Embedded shift register mode	Support
ROM mode	Support
FIFO buffer	Support
Simple dual-port mixed width support	Support
True dual-port mixed width support	Support
Memory initialization file	Support
Mixed-clock mode	Support
Power-up condition	Outputs cleared
Register asynchronous clears	Read address registers and output registers only
Latch asynchronous clears	Output latches only
Write or read operation triggering	Write and read: Rising clock edges
Same-port read-during-write	Outputs set to **Old Data** or **New Data**
Mixed-port read-during-write	Outputs set to **Old Data** or **Don't Care**

AGM SoC FPGA devices M9K memory blocks allow you to implement fully-synchronous SRAM memory in multiple modes of operation. M9K memory blocks do not support asynchronous (unregistered) memory inputs. M9K memory blocks support the following modes:

Single-port, Simple dual-port, True dual-port, Shift-register, ROM, FIFO

6.8. Embedded Multipliers

AGM SoC FPGA devices include a combination of on-chip resources that help increase performance, reduce system cost, and lower the power consumption of digital signal processing (DSP) systems. AGM SoC FPGA devices, either alone or as DSP device co-processors, are used to improve price-to-performance ratios of DSP systems. Particular focus is placed on optimizing AGM SoC FPGA devices for applications that benefit from an abundance of parallel processing resources, which include video and image processing, wireless communications, and multi-channel communications and video systems.

The embedded multiplier is configured as either one 18 × 18 multiplier or two 9 × 9 multipliers. For multiplications greater than 18 × 18, the AGM software cascades multiple embedded multiplier blocks together. There are no restrictions on the data width of the multiplier, but the greater the data width, the slower the multiplication process.

You can use an embedded multiplier block in one of two operational modes, depending on the application needs:

- One 18 × 18 multiplier
- Up to two 9 × 9 independent multipliers

You can also use embedded multipliers of AGM SoC FPGA devices to implement multiplier adder and multiplier accumulator functions, in which the multiplier portion of the function is implemented with embedded multipliers, and the adder or accumulator function is implemented in logic elements (LEs).

6.9. I/O

AGM SoC FPGA architectrue support these I/O features:

- Supports 3.3-V, 2.5-V, 1.8-V, and 1.5-V logic levels: LVTTL, LVCMOS
- Programmable drive strength, bus-hold, pull-up resistors, open-drain output, input and output delay, slew rate control.
- Differential I/O standards: LVPECL, True-LVDS, RSDS, Mini-LVDS, BLVDS.

I/O pins on AGM SoC FPGA devices are grouped together into I/O banks. Each bank has a separate power bus. AGM SoC FPGA devices have eight I/O banks. Each device I/O pin is associated with one I/O bank. All single-ended and differential I/O standards are supported in all banks. All differential I/O standards are supported in all banks.

AGM SoC FPGA devices can send and receive data through LVDS signals. For the LVDS transmitter and receiver, the input and output pins of devices support serialization and deserialization through internal logic.

The BLVDS extends the benefits of LVDS to multipoint applications such as bidirectional backplanes. The loading effect and the need to terminate the bus at both ends for multipoint applications require BLVDS to drive out a higher current than LVDS to produce a comparable voltage swing. All the I/O banks support BLVDS for user I/O pins.

The RSDS and mini-LVDS standards are derivatives of the LVDS standard. The RSDS and mini-LVDS I/O standards are similar in electrical characteristics to LVDS, but have a smaller voltage swing and therefore provide increased power benefits and reduced electromagnetic interference (EMI).

The LVDS standard does not require an input reference voltage, but it does require a 100-ohm termination resistor between the two signals at the input buffer. An external resistor network is required on the transmitter side for the top and bottom I/O banks.

6.10. External Memory Interfaces

AGM SoC FPGA architecture can easily interface with a broad range of external memory devices, including DDR2 SDRAM, DDR SDRAM, and QDR II SRAM. External memory devices are an important system component of a wide range of image processing, storage, communications, and general embedded applications.

AG6KMCUSoC FPGA devices use data (DQ), data strobe (DQS), clock, command, and address pins to interface with external memory.

7. Device Configuration

7.1. Configuration Flow

AGM SoC device store the configuration data in the internal spi flash. The stored configuration files contain MCU configuration file and FPGA configuration file. After the device power is up, the FPGA configuration file is loaded first and then MCU init configuration logic load MCU configuration file from the specified address of the internal spi flash.

7.2. Configuration Data Compression

AGM FPGA configuration file support configuration data decompression, which saves configuration memory space and time. This feature allows you to store compressed configuration data in configuration devices or other memory and send the compressed bitstream to AGM FPGA devices. During configuration, AGM FPGA devices decompress the bitstream in real time and program the SRAM cells.

When you enable compression, the AGM software generates configuration files with compressed configuration data. This compressed file reduces the storage requirements in the configuration device or flash memory and decreases the time required to send the bitstream to the AGM FPGA device.

8. DC Electrical Characteristics

8.1. Power-On Reset Circuitry

When power is applied to AGM SoC devices, the POR circuit monitors V_{CC} and begins SRAM download at an approximate voltage of 1.2V AGM SoC devices.

Entry into user mode is gated by whether V_{CCIO} bank are powered with sufficient operating voltage. If V_{CC} and V_{CCIO} are powered simultaneously, the device enters user mode.

For AGM SoC when in user mode, the POR circuitry continues to monitor the V_{CC}(but not V_{CCIO}) voltage level to detect a brown-out condition. If there is a V_{CC} voltage sag at during user mode, the POR circuit resets the SRAM and tri-states the I/O pins. Once V_{CC} rises back to approximately 1.2V, the SRAM download restarts and the device begins to operate.

The below tables are the AGM SoC power electrical characteristics.

Table 8-1 Absolute Maximum Ratings for AGM FPGA Devices

Symbol	Parameter	Min	Max	Unit
V_{CCINT}	Core voltage	–0.5	1.8	V
V_{CCA}	Phase-locked loop (PLL) analog power supply	–0.5	3.75	V
V_{CCD_PLL}	PLL digital power supply	–0.5	4.5	V
V_{CCIO}	I/O banks power supply	–0.5	3.75	V
V_{CC_CLKIN}	Differential clock input pins power supply	–0.5	4.5	V
V_I	DC input voltage	–0.5	4.2	V
I_{OUT}	DC output current, per pin	–25	40	mA
T_{STG}	Storage temperature	–65	150	°C
T_J	Operating junction temperature	–40	100	°C

Table 8-2. Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CCINT}	Supply voltage for internal logic, 1.2V operation	-	1.15	1.2	1.25	V
V_{CCIO}	Supply voltage for output buffers, 3.3-V operation	-	3.135	3.3	3.465	V
	Supply voltage for output buffers, 2.5-V operation	-	2.375	2.5	2.625	V
	Supply voltage for output buffers, 1.8-V operation	-	1.71	1.8	1.89	V
	Supply voltage for output buffers, 1.5-V operation	-	1.425	1.5	1.575	V

V_{CCA}	Supply (analog) voltage for PLL regulator	-	2.375	2.5	2.625	V
V_{CCD_PLL}	Supply (digital) voltage for PLL, 1.2-V operation	-	1.15	1.2	1.25	V
V_I	Input voltage	-	-0.5	-	3.6	V
V_O	Output voltage	-	0	-	VCCIO	V
T_J	Operating junction temperature	For commercial use	0	-	85	°C
		For industrial use	-40	-	100	°C
t_{RAMP}	Power supply ramp time	Standard power-on reset (POR)	50 μs	-	50 ms	-
		Fast POR	50 μs	-	3 ms	-

Table 8-3. I/O Pin Leakage Current

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_I	Input pin leakage current	V_I = 0 V to $V_{CCIOMAX}$	-10	-	10	μA
I_{OZ}	Tristated I/O pin leakage current	V_O = 0 V to $V_{CCIOMAX}$	-10	-	10	μA

Table 8-4. Single-Ended I/O Standard Specifications

I/O Standard	V_{CCIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (mA)	I_{OH} (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
3.3-V LVTTL	3.135	3.3	3.465	-	0.8	1.7	3.6	0.45	2.4	4	-4
3.3-V LVCMOS	3.135	3.3	3.465	-	0.8	1.7	3.6	0.2	V_{CCIO} -0.2	2	-2
2.5 V	2.375	2.5	2.625	-0.3	0.7	1.7	V_{CCIO} +0.3	0.4	2.0	1	-1
1.8 V	1.71	1.8	1.89	-0.3	0.35 x V_{CCIO}	0.65 x V_{CCIO}	2.25	0.45	V_{CCIO} -0.45	2	-2
1.5 V	1.425	1.5	1.575	–0.3	0.35 x V_{CCIO}	0.65 x V_{CCIO}	V_{CCIO} +0.3	0.25 x V_{CCIO}	0.75 x V_{CCIO}	2	-2

Table 8-5. Differential I/O Standard Specifications

I/O Standard	V_{CCIO} (V)			V_{ID} (mV)		V_{ICM} (V)		
	Min	Typ	Max	Min	Max	Min	Condition	Max
LVPECL	2.375	2.5	2.625	100	-	0.05	$D_{MAX} \leq$ 500 Mbps	1.80
						0.55	500 Mbps $\leq D_{MAX} \leq$ 700 Mbps	1.80
						1.05	D_{MAX} > 700 Mbps	1.55
LVDS	2.375	2.5	2.625	100	-	0.05	$D_{MAX} \leq$ 500 Mbps	1.80
						0.55	500 Mbps $\leq D_{MAX} \leq$ 700 Mbps	1.80
						1.05	D_{MAX} > 700 Mbps	1.55

I/O Standard	V_{CCIO} (V)			V_{ID} (mV)		V_{OD} (mV)			V_{OS} (V)		
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max
LVDS	2.375	2.5	2.625	100	-	247	-	600	1.125	1.25	1.375
BLVDS	2.375	2.5	2.625	100	-	-	-	-	-	-	-
mini-LVDS	2.375	2.5	2.625	-	-	300	-	600	1.0	1.2	1.4
RSDS	2.375	2.5	2.625	-	-	100	200	600	0.5	1.2	1.5

9. System Address

9.1. Address Map

The comprehensive system level address map is shown in Table 9-1. The shaded entries indicate that the address range is reserved and should not be accessed.

Table 9-1 System Address Map

TBD

9.2. Registers

TBD

10. Pin-Outs

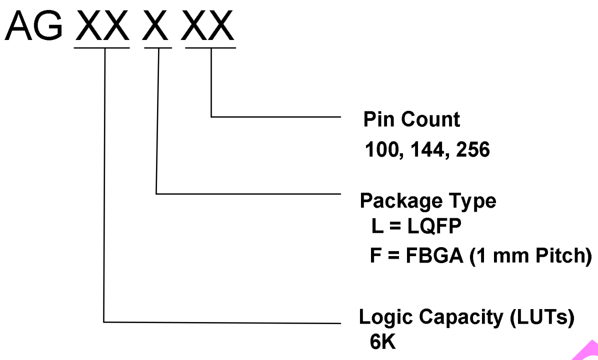
Refer to Pin-Outs printouts for AGM SoC device family.

11. Software

AGM Software tools support from RTL to bit stream configuration implementation and programming. Supported operating system platforms include Microsoft Windows and Linux.

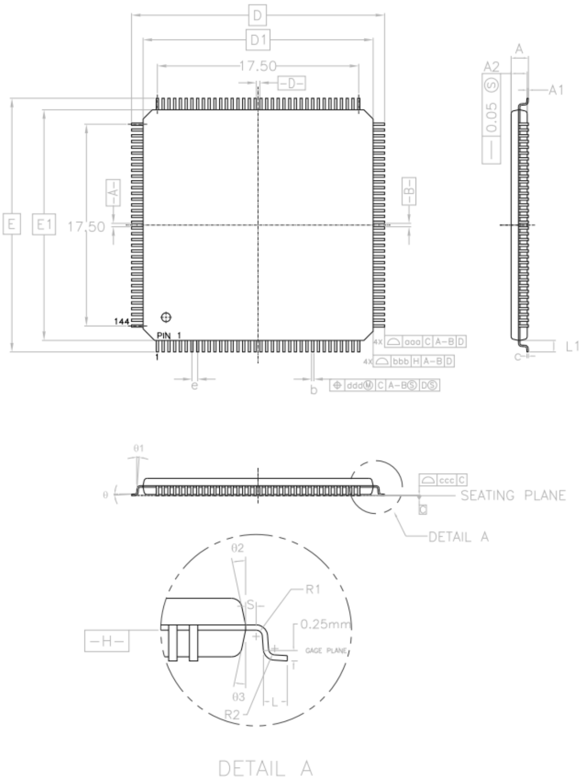
12. Ordering Information

Table12-1 Device Part Number Description



13. Package

LQFP-100



FOR CUSTOMER ONLY				
PACKAGE TYPE	EP LQFP			
DESCRIPTION	SYMBOL	MILLIMETER		
		MIN	NOM	MAX
TOTAL THICKNESS	A	–	–	1.60
STAND OFF	A1	0.05	–	0.15
TOTAL MOLD THICKNESS	A2	1.35	1.40	1.45
PACKAGE SIZE WITH LEAD	D	–	22 BSC	–
	E	–	22 BSC	–
PACKAGE SIZE	D1	–	20 BSC	–
	E1	–	20 BSC	–
EP SIZE	D3	–	9.74 BSC	–
	E3	–	9.74 BSC	–
LEAD TURN RADIUS	R1	0.08	–	–
LEAD TURN RADIUS	R2	0.08	–	0.20
LEAD TURN ANGLE	θ	0°	3.5°	7°
LEAD TURN ANGLE	θ1	0°	–	–
LEAD TURN ANGLE	θ2	11°	12°	13°
LEAD TURN ANGLE	θ3	11°	12°	13°
LEAD CONTACT LENGTH	L	0.45	0.60	0.75
LEAD LENGTH	L1	–	1.00	–
MATERIAL THICKNESS	c	0.09	–	0.20
LEAD SPAN LENGTH	S	0.20	–	–

PIN COUNT	144			
DESCRIPTION	SYMBOL	MILLIMETER		
		MIN	NOM	MAX
LEAD PITCH	e		0.50 BSC	
LEAD WIDTH	b	0.17	0.20	0.27
LEAD EDGE PROFILE	aaa		0.20	
PACKAGE EDGE PROFILE	bbb		0.20	
LEAD COPLANARITY	ccc		0.08	
LEAD POSITION OFFSET	ddd		0.08	

14. Recommended Reflow Profile

Figure. 14-1 Classification Reflow Profile

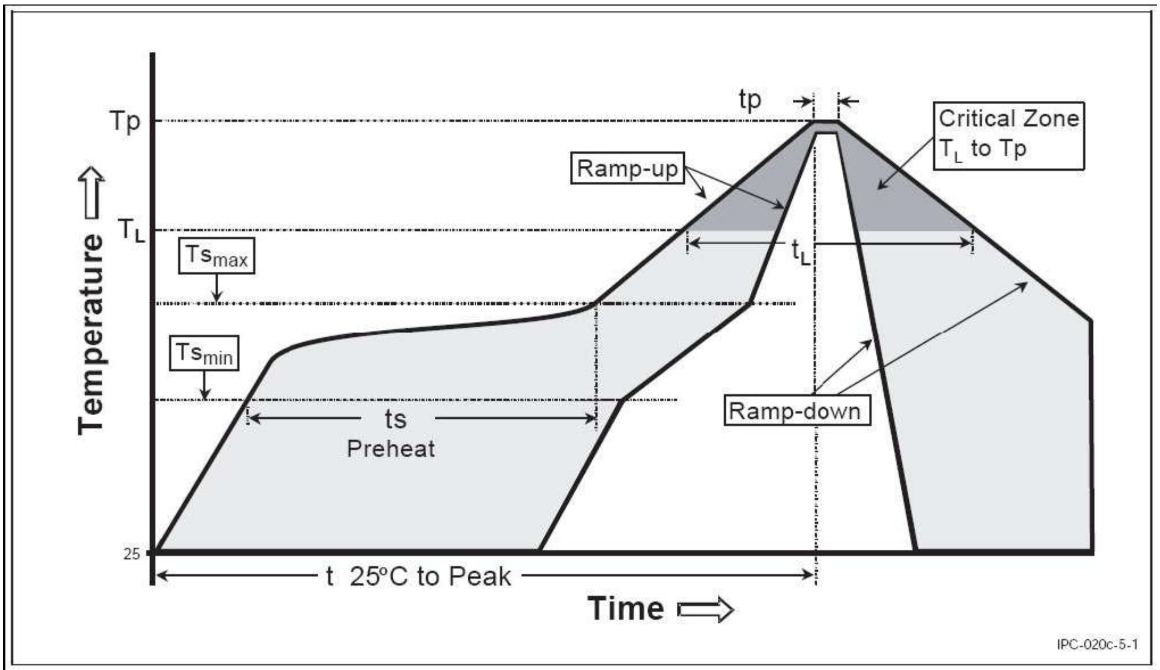


Table 14-1 Classification Reflow Profiles

Profile Feature	**Sn-Pb Eutectic Assembly**	**Pb-Free Assembly**
Average Ramp-Up Rate (TSmax to Tp)	3 ℃/second max.	3 ℃/second max.
Preheat -Temperature Min (Tsmin) -Temperature Max (Tsmax) -Time (tsmin to tsmax)	 100 ℃ 100 ℃ 60-120 seconds	 150 ℃ 200 ℃ 60-180 seconds
Time maintained above: -Temperature (TL) -Time (tL)	 183 ℃ 60-150seconds	 217℃ 60-150 seconds
Peak /Classification Temperature(Tp)	See Table 10	See Table 11
Time within 5 oC of actual Peak Temperature (tp)	10-30 seconds	20-40 seconds
Ramp-Down Rate	6 ℃/second max.	6 ℃/seconds max.
Time 25 oC to Peak Temperature	6 minutes max.	8 minutes max.

Table 14-2 Sn-Pb Eutectic Process – Package Peak Reflow Temperatures

Package Thickness	Volume mm3 <350	Volume mm3 ≥350
＜2.5mm	240 + 0/-5 ℃	225 + 0/-5 ℃
≥2.5mm	225 + 0/-5 ℃	225 + 0/-5 ℃

Table 14-3 Pb-free Process – Package Classification Reflow Temperatures

Package Thickness	Volume mm3 ＜350	Volume mm3 350-2000	Volume mm3 ＞2000
＜1.6mm	260 + 0 ℃ *	260 + 0 ℃ *	260 + 0 ℃ *
1.6mm – 2.5mm	260 + 0 ℃ *	250 + 0 ℃ *	245 + 0 ℃ *
≥2.5mm	250 + 0 ℃ *	245 + 0 ℃ *	245 + 0 ℃ *
*Tolerance : The device manufacturer/supplier shall assure process compatibility up to and including the stated classification temperature(this mean Peak reflow temperature + 0 ℃. For example 260+ 0 ℃) at the rated MSL Level.			

Note 1: All temperature refer topside of the package. Measured on the package body surface.

Note 2: The profiling tolerance is + 0 ℃, - X ℃ (based on machine variation capability)whatever is required to control the profile process but at no time will it exceed – 5 ℃. The producer assures process compatibility at the peak reflow profile temperatures defined in Table 9-3.

Note 3: Package volume excludes external terminals(balls, bumps, lands, leads) and/or non integral heat sinks.

Note 4: The maximum component temperature reached during reflow depends on package the thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD package may sill exist.

Note 5: Components intended for use in a "lead-free" assembly process shall be evaluated using the "lead free" classification temperatures and profiles defined in Table8-1, 8-2, 8-3 whether or not lead free.

15. Change List

The following table summarizes revisions to this document.

REV	DATE	AUTHER	CHANGE DESCRIPTION
V1.0	02/11/2018		Release Version 1.0

16. RoHS Compliant

The product does not contain lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB) or polybrominated diphenyl ethers (PBDE), and are therefore considered RoHS compliant.

17. ESD Precautions

ESD protection circuitry is contended in this device, but special handling precautions are required.